

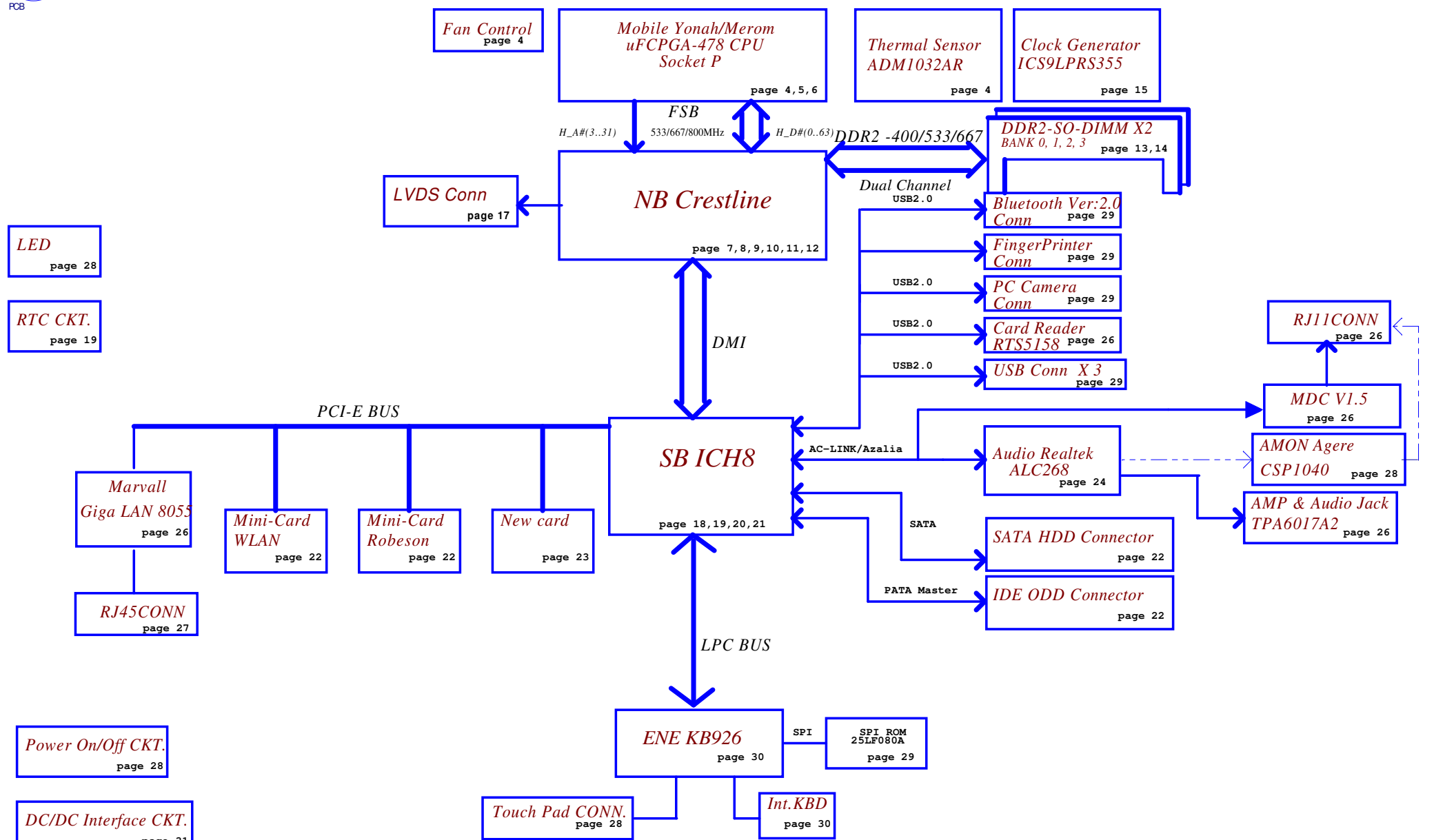
# Compal confidential

## Schematics Document

### Mobile Merom uFCPGA with Satna Rosa Platform

2007-07-24  
REV:0.3

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## Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +1.25VS +0.9V +VCCP +CPU_CORE
S0	○	○	○	○
S1	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

### Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.

## I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

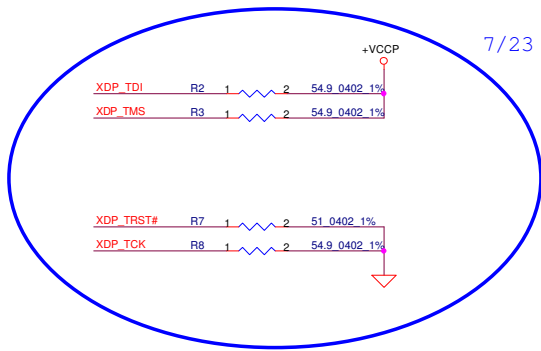
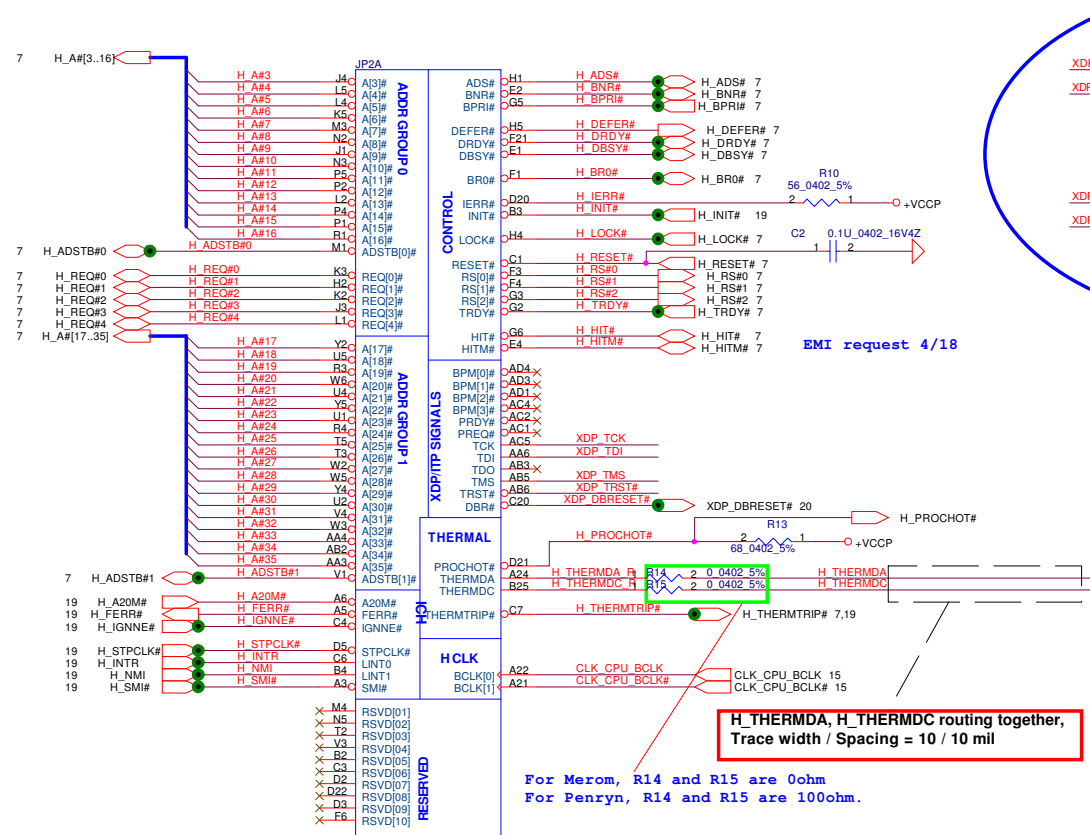
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU) ADM1032	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB925	✗	✓	✓	✗	✗	✗	✗	✗
SMB_EC_CK2 SMB_EC_DA2	KB925	✗	✗	✗	✓	✗	✗	✗	✗
SMB_CK_CLK1 SMB_CK_DAT1	ICH8	✗	✗	✗	✗	✓	✓	✓	✗
LCD_CLK LCD_DAT	Crestline	✗	✗	✗	✗	✗	✗	✗	✓

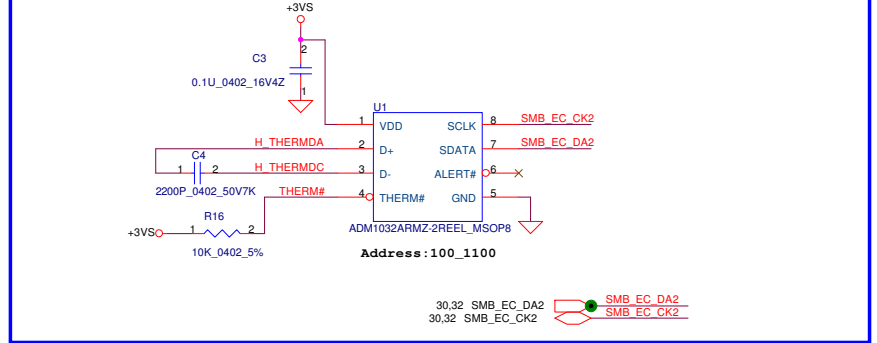
BOM: 43XXXXXX

Jump-Short: PJP?

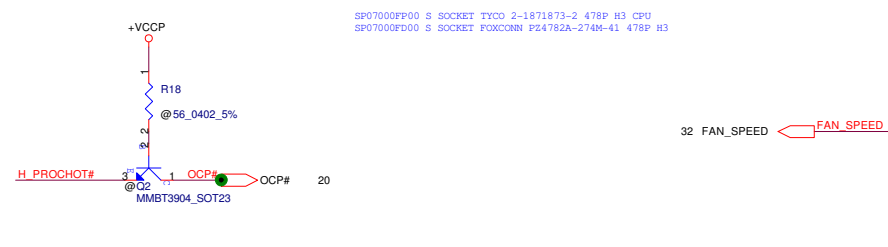
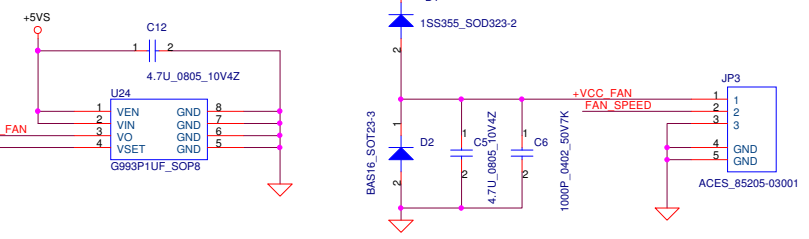
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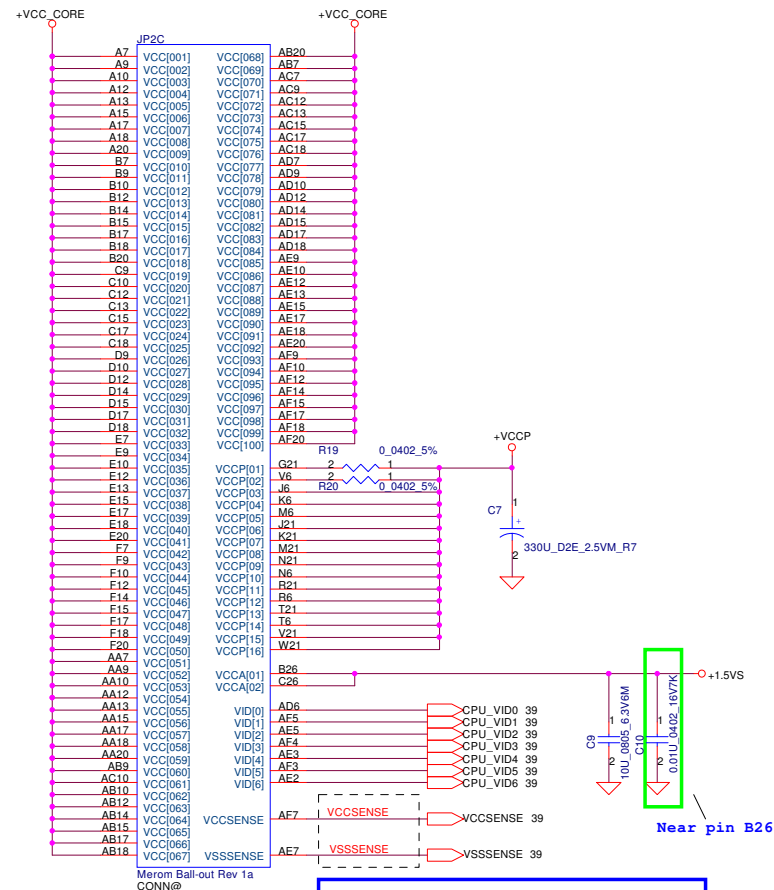
### Thermal Sensor ADM1032ARMZ



### Voltage Fan Control circuit



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Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

Close to CPU pin AD26  
within 500mils.

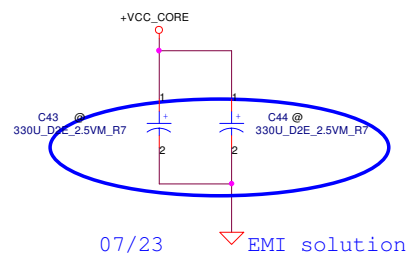
Length match within 25 mils.  
The trace width/space/other is  
20/7/25.

Close to CPU pin  
within 500mils.

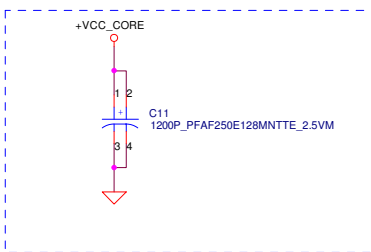
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JP20		
A4	VSS[001]	P6
A8	VSS[002]	P21
A11	VSS[003]	P24
A14	VSS[004]	R2
A16	VSS[005]	R5
A19	VSS[006]	R22
A23	VSS[007]	R25
AF2	VSS[008]	T1
B6	VSS[009]	T4
B8	VSS[010]	T23
B11	VSS[011]	T26
B13	VSS[012]	U3
B16	VSS[013]	U6
B19	VSS[014]	U21
B21	VSS[015]	U24
B24	VSS[016]	V2
C5	VSS[017]	V5
C8	VSS[018]	V22
C11	VSS[019]	V25
C14	VSS[020]	W1
C16	VSS[021]	W4
C19	VSS[022]	W23
C2	VSS[023]	W26
C22	VSS[024]	Y3
C25	VSS[025]	Y6
D1	VSS[026]	Y21
D4	VSS[027]	Y24
D8	VSS[028]	AA2
D13	VSS[029]	AA5
D16	VSS[030]	AA11
D19	VSS[031]	AA14
D23	VSS[032]	AA16
D26	VSS[033]	AA19
E3	VSS[034]	AA22
E6	VSS[035]	AA25
E8	VSS[036]	AB1
E11	VSS[037]	AB4
E14	VSS[038]	AB8
E16	VSS[039]	AB11
E19	VSS[040]	AB13
E21	VSS[041]	AB16
E24	VSS[042]	AB19
F5	VSS[043]	AB23
F8	VSS[044]	AB26
F11	VSS[045]	AC3
F13	VSS[046]	AC6
F16	VSS[047]	AC8
F19	VSS[048]	AC11
F2	VSS[049]	AC14
F22	VSS[050]	AC16
F25	VSS[051]	AC19
G4	VSS[052]	AC21
G1	VSS[053]	AC24
G23	VSS[054]	AD2
G26	VSS[055]	AD5
H3	VSS[056]	AD8
H6	VSS[057]	AD11
H21	VSS[058]	AD13
H24	VSS[059]	AD16
J2	VSS[060]	AD19
J5	VSS[061]	AD22
J22	VSS[062]	AD25
J25	VSS[063]	AE1
K1	VSS[064]	AE4
K23	VSS[065]	AE8
K26	VSS[066]	AE11
L3	VSS[067]	AE14
L6	VSS[068]	AE16
L21	VSS[069]	AE19
L24	VSS[070]	AE23
M2	VSS[071]	AE26
M5	VSS[072]	A2
M22	VSS[073]	AF6
M25	VSS[074]	AF8
N1	VSS[075]	AF11
N4	VSS[076]	AF13
N23	VSS[077]	AF16
N26	VSS[078]	AF19
P3	VSS[079]	AF21
	VSS[080]	A25
	VSS[081]	AF25
	VSS[082]	

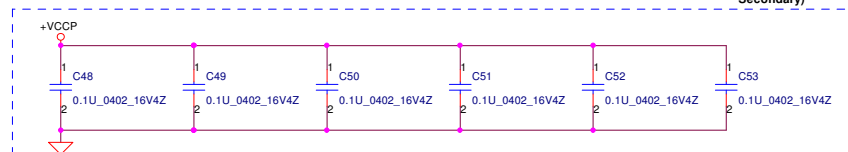
## Near CPU CORE regulator



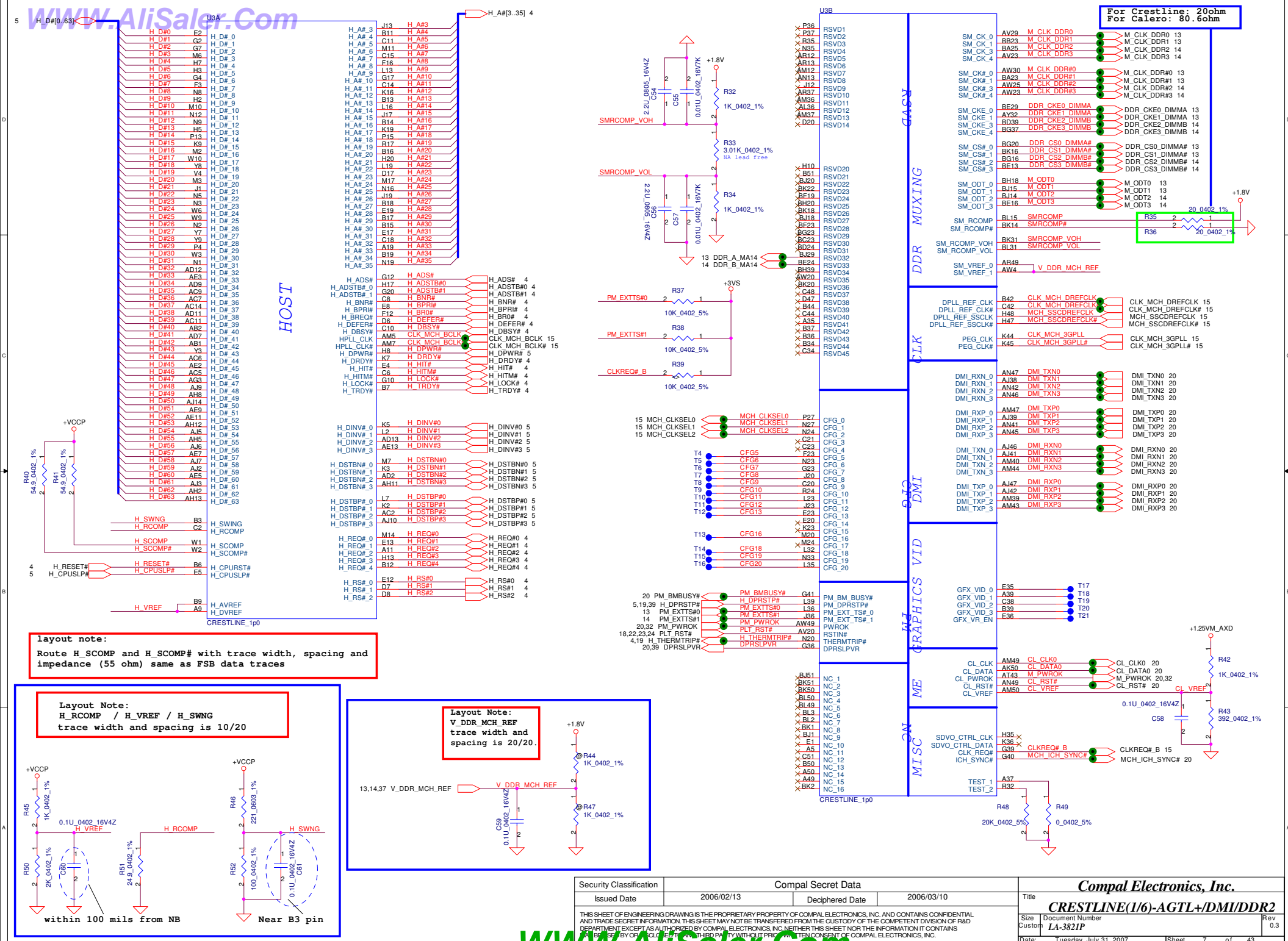
## Proadlizer



Place these inside  
socket cavity on L8  
(North side  
Secondary)

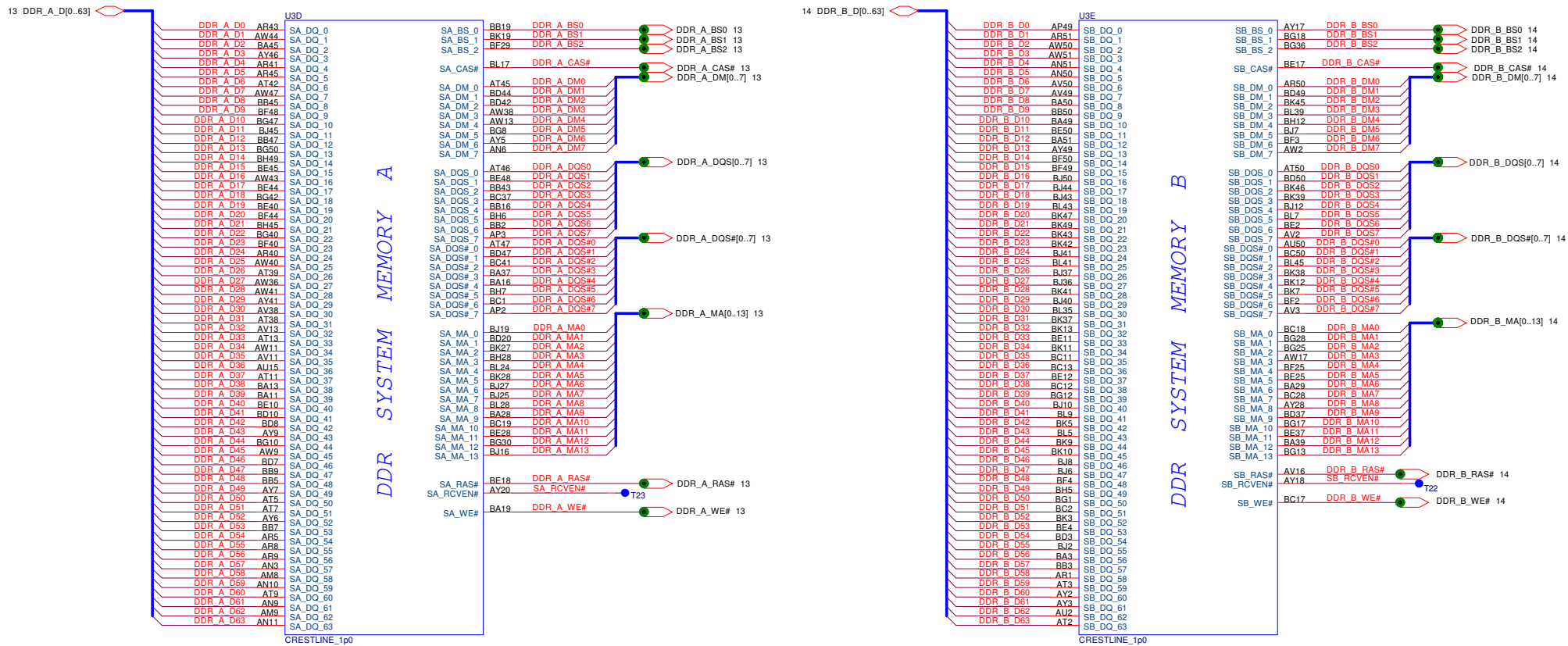


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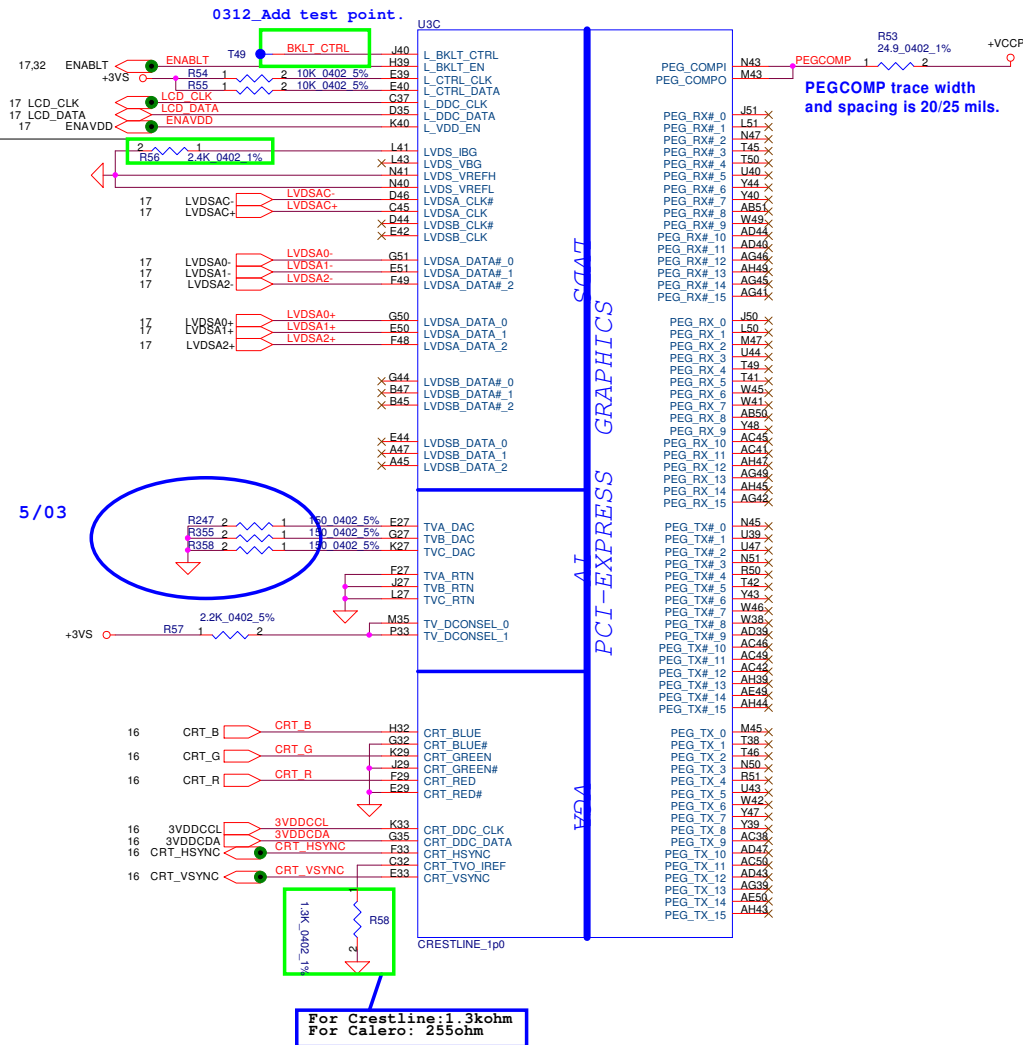




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For Crestline: 2.4kohm  
For Calero: 1.5kohm



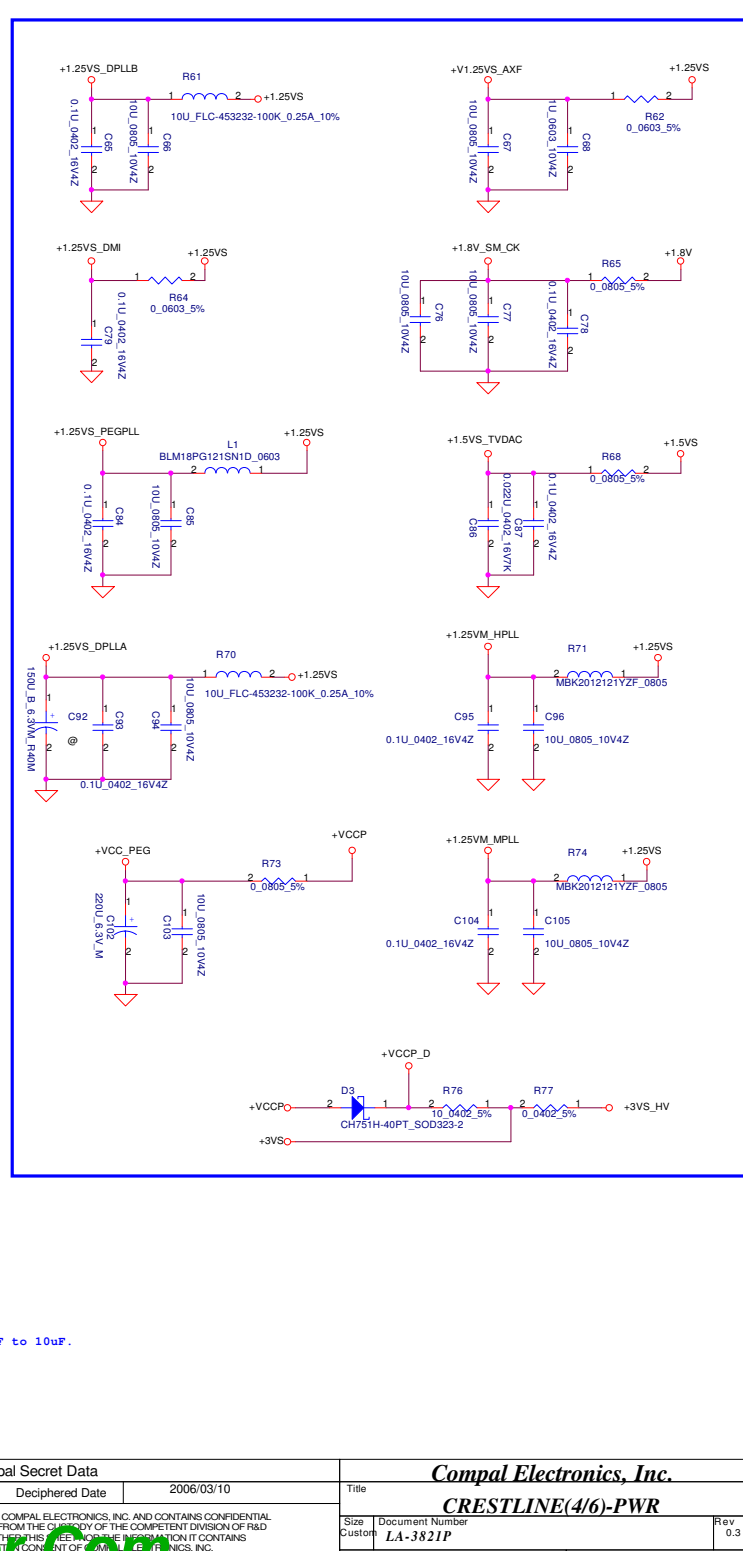
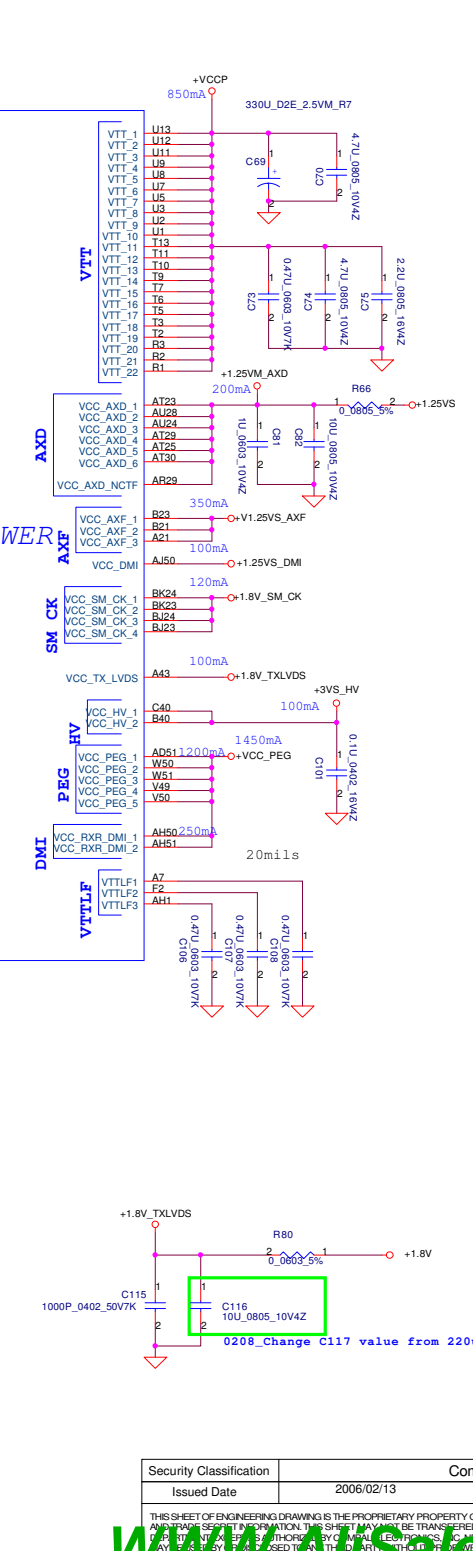
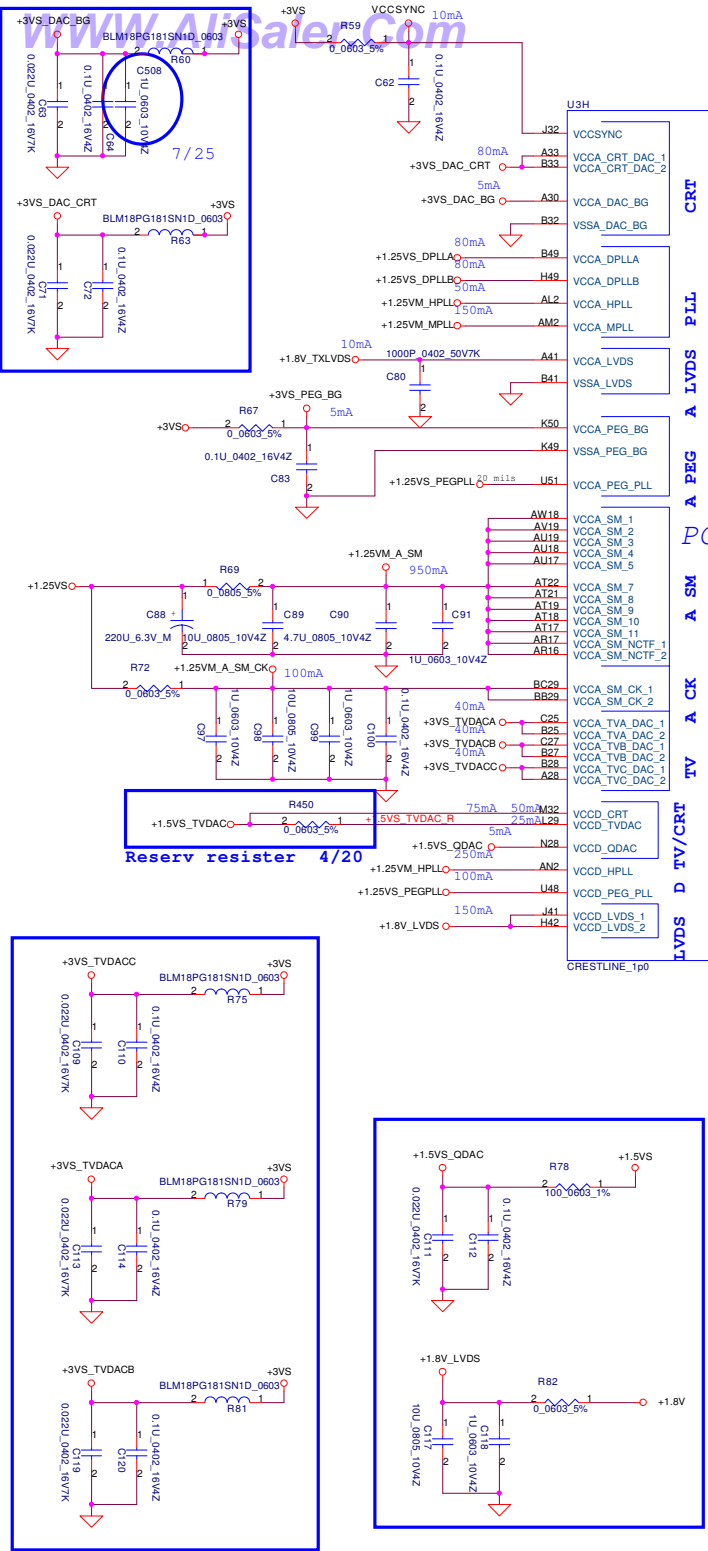
Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

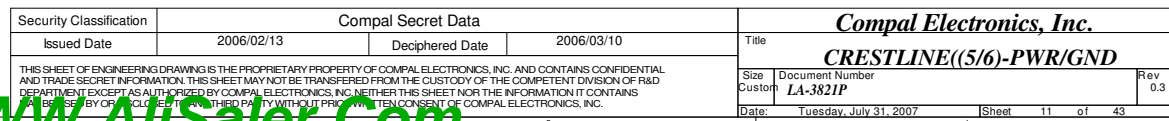
CFG[17:3] have internal pull up

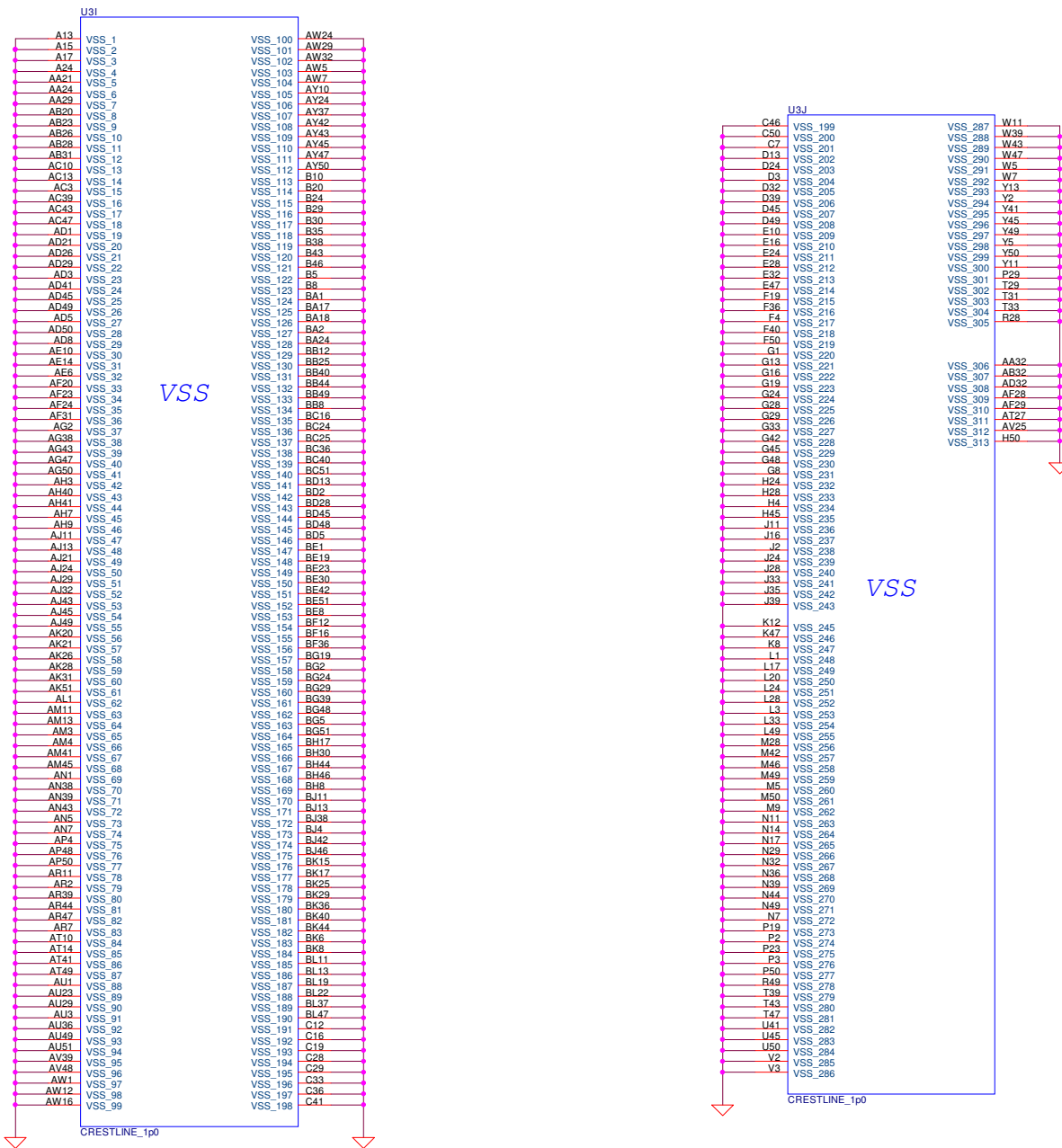
CFG[19:18] have internal pull down

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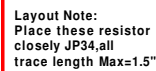
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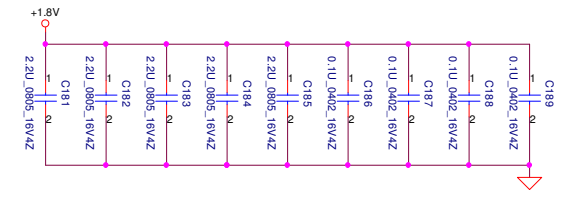
The diagram illustrates a power plane for a 1.8V supply. A horizontal line at the top is labeled +1.8V. A series of capacitors, labeled C154 through C159, are connected in parallel between this supply line and a common ground plane. The capacitors are arranged in a row, with their positive terminals connected to the +1.8V line and their negative terminals connected to the ground plane. The ground plane is represented by a horizontal line at the bottom, with a red triangle indicating a connection point. The capacitors are labeled as follows: C154 (330U\_4V\_M), C155 (220\_0005\_16V4Z), C156 (220\_0005\_16V4Z), C157 (220\_0005\_16V4Z), C158 (220\_0005\_16V4Z), C159 (0.1U\_0402\_16V4Z), C160 (0.1U\_0402\_16V4Z), C161 (0.1U\_0402\_16V4Z), C162 (0.1U\_0402\_16V4Z), C163 (0.1U\_0402\_16V4Z), and C164 (0.1U\_0402\_16V4Z).



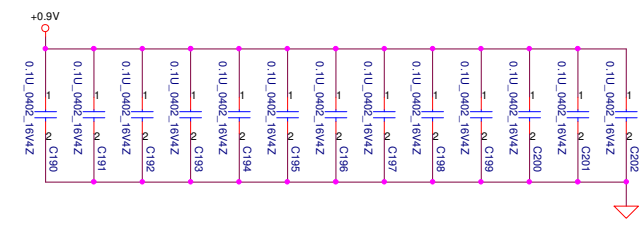
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8 DDR\_B\_DQS#0[0..7]  
8 DDR\_B\_D[0..63]  
8 DDR\_B\_DM[0..7]  
8 DDR\_B\_DQS#0[0..7]  
7,8 DDR\_B\_MA[0..14]

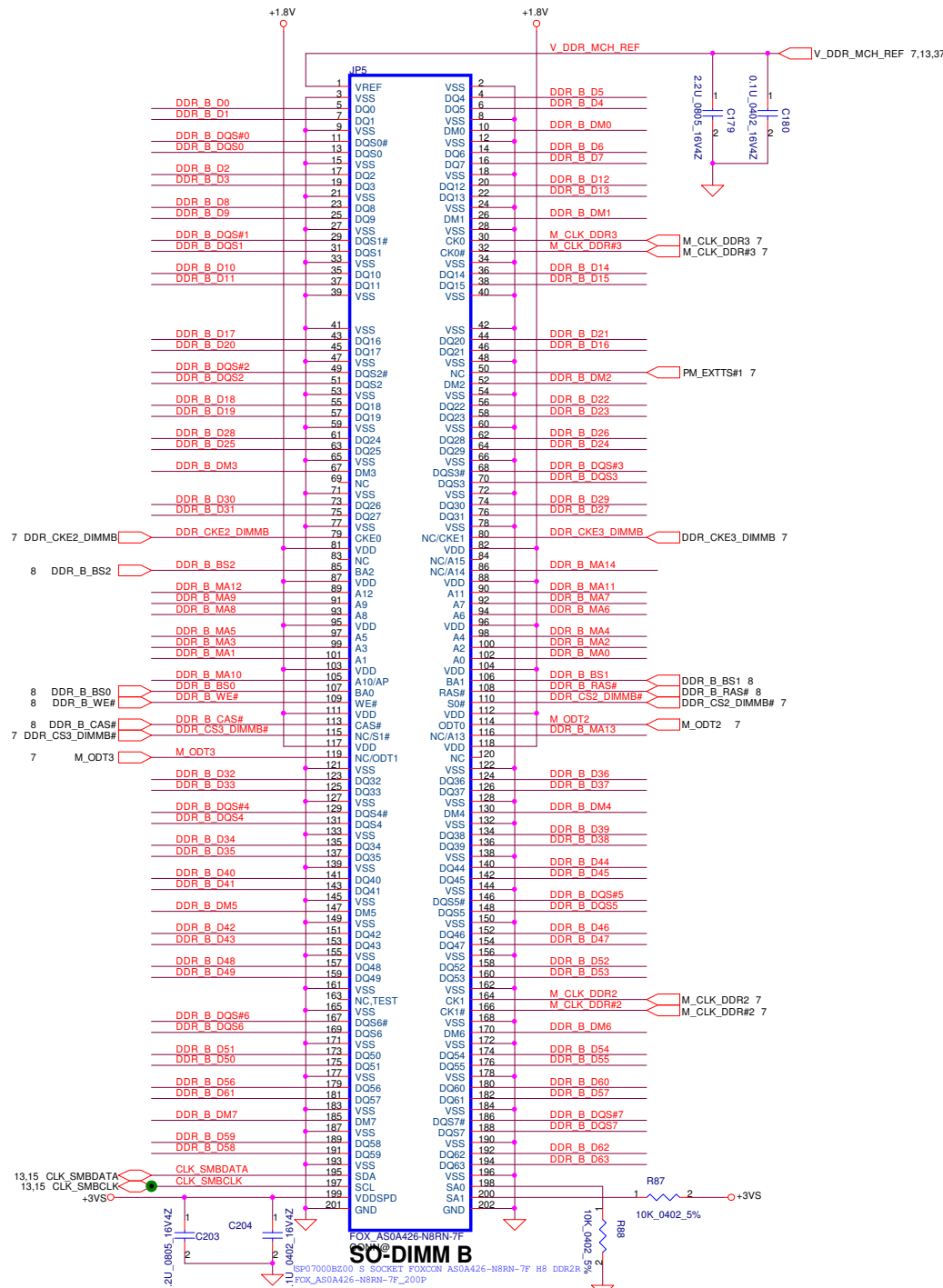
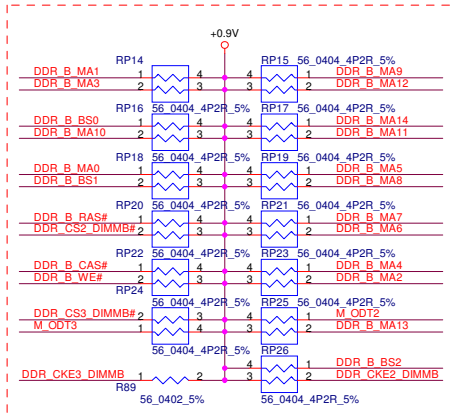
Layout Note:  
Place near JP10



Layout Note:  
Place one cap close to every 2 pullup resistors terminated to +0.9V



Layout Note:  
Place these resistor closely JP10, all trace length Max=1.5"



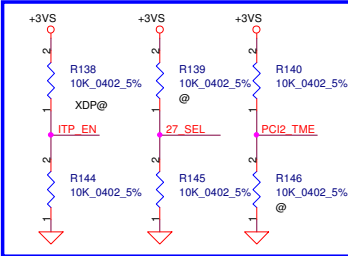
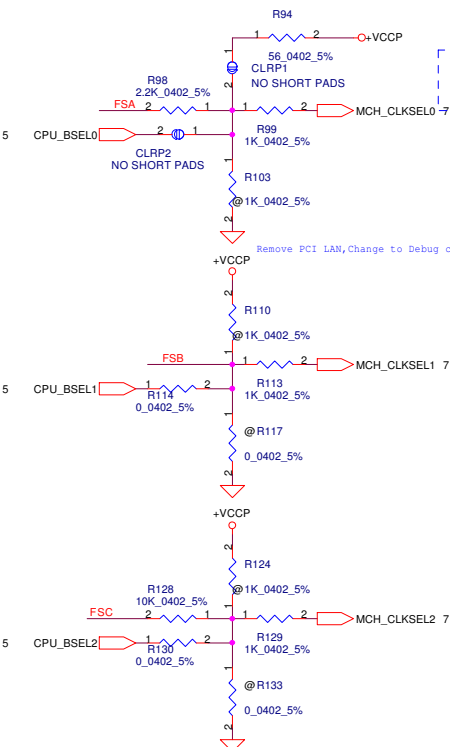
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FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

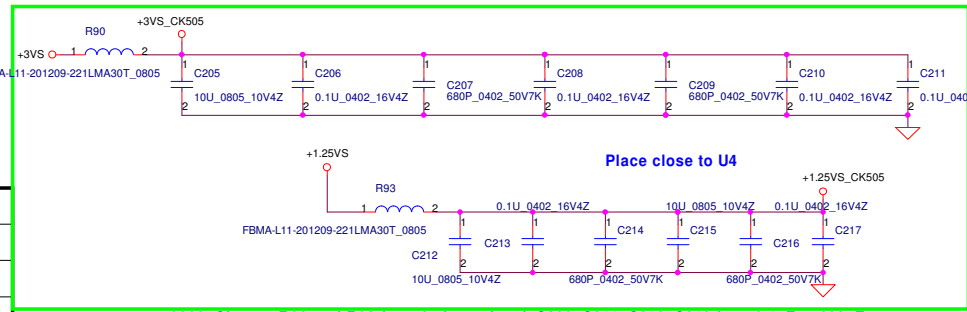
#### FSB Frequency Selet:

CPU Driven	Stuff	R1107	R1135	R1083
* (Default)	No Stuff	R1074	R1086	R1098
		R1113	R1128	R1139
		R1086	R1139	R1135
		R1083	R1107	R1128
		R1113	R1098	
667MHz	Stuff	R1086	R1139	R1135
	No Stuff	R1083	R1107	R1128
		R1113	R1098	
800MHz	Stuff	R1135	R1139	
	No Stuff	R1083	R1086	R1098
		R1074	R1107	R1113

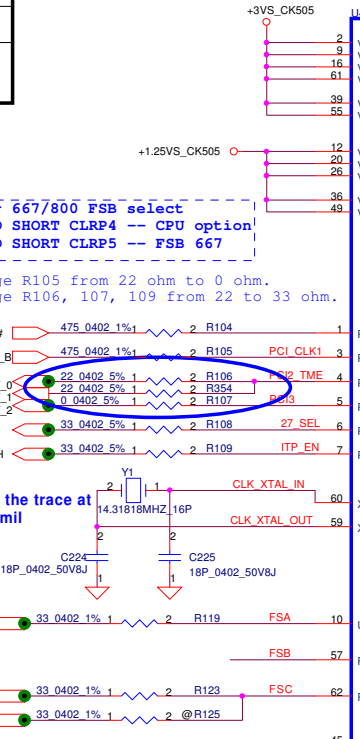


For ITP\_EN, 0 = SRC8/SRC8#; 1 = ITP/ITP#  
 For 27\_SEL, 0 = Enable DOT96 & SRC1,  
 1 = Enable SRC0 & 27MHz  
 For PCI2\_EN, 0 = Overclocking of CPU and SRC Allowed  
 1 = Overclocking of CPU and SRC NOT allowed

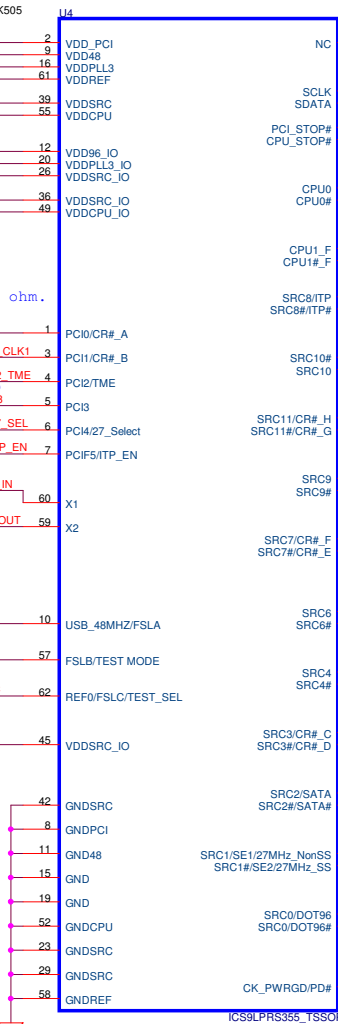
For Layout request:  
 1. Change MINI\_CLKREQ# from pin 32 to pin 43.  
 2. Change CLK\_PCIE\_MCARD from SRC9 to SRC6.



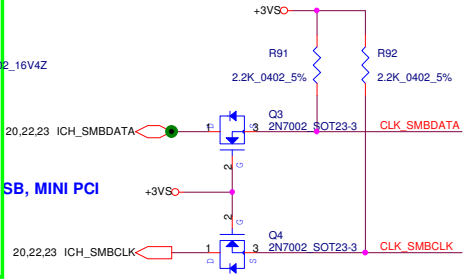
0308\_Change R89 and R92 form 0 ohm to bead, C209, C211, C216, C218 from 0.1uF to 680pF.



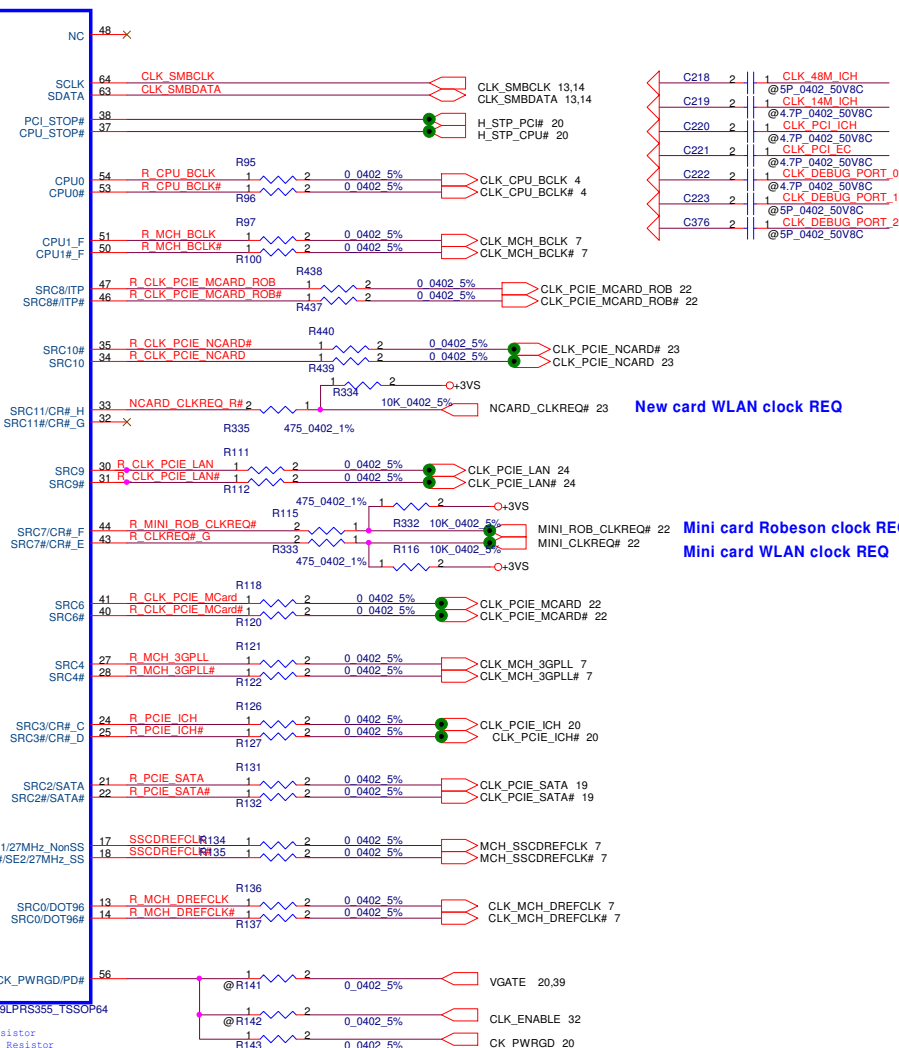
Routing the trace at least 10mil



\* Internal Pull-Up Resistor  
 \*\* Internal Pull-Down Resistor



SB, MINI PCI

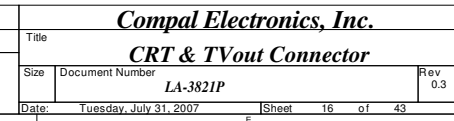


New card WLAN clock REQ

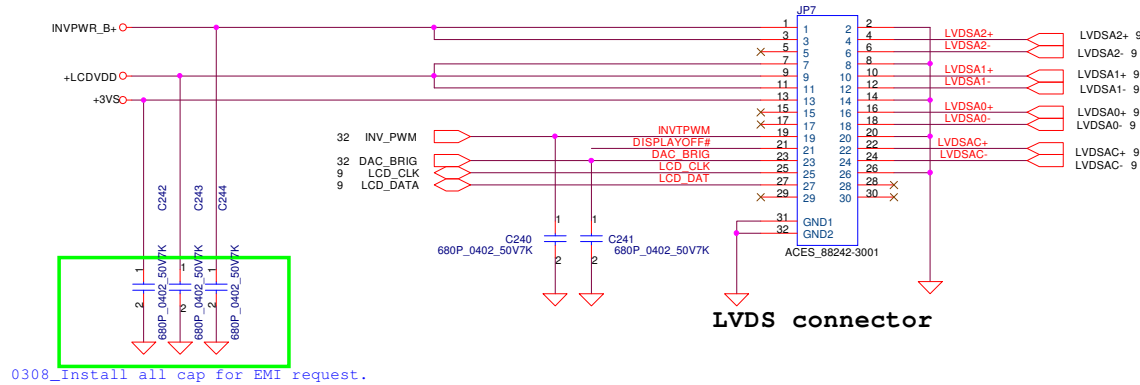
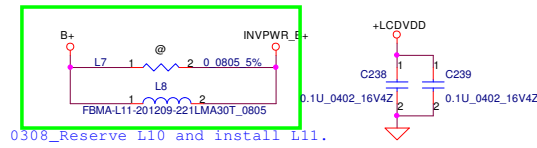
Mini card Robeson clock REQ  
 Mini card WLAN clock REQ

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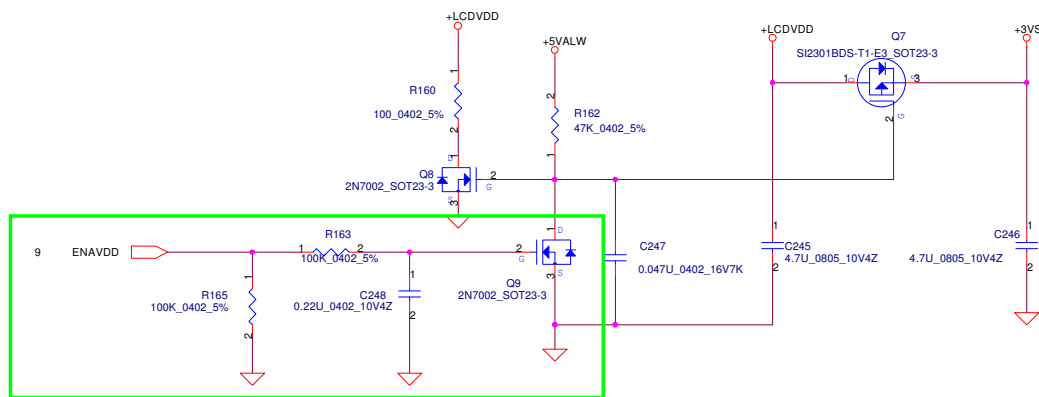
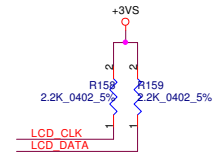




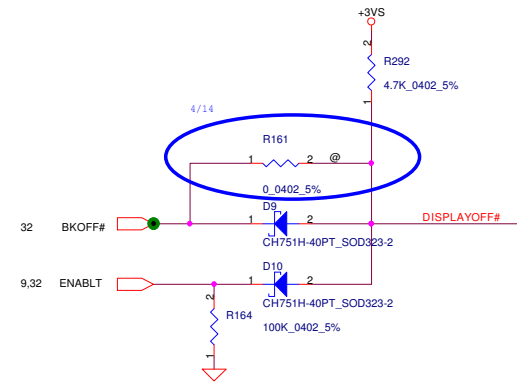
# LVDS CONN



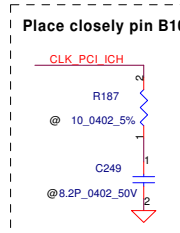
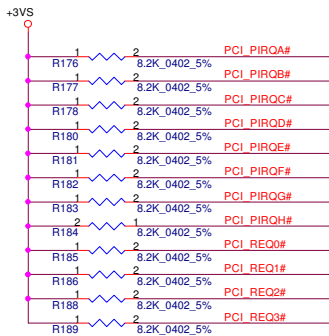
LVDS connector



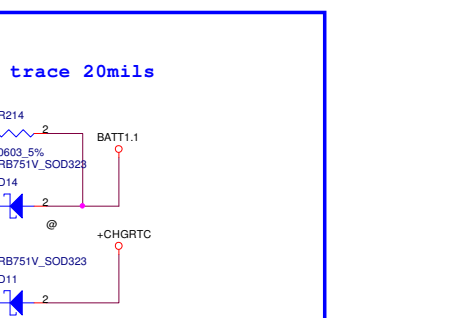
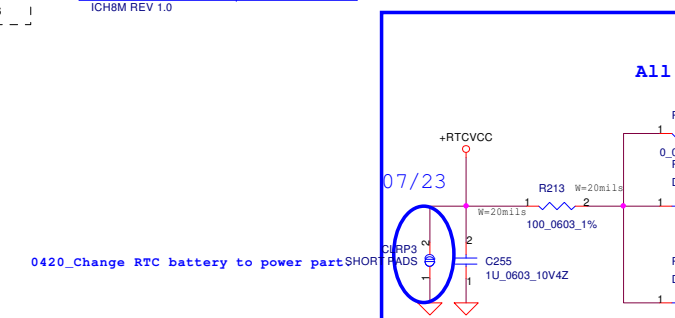
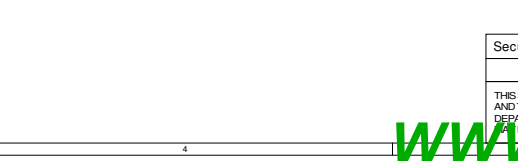
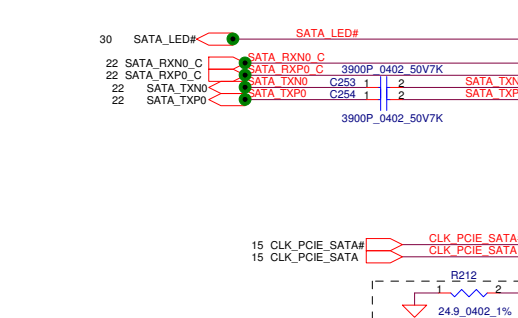
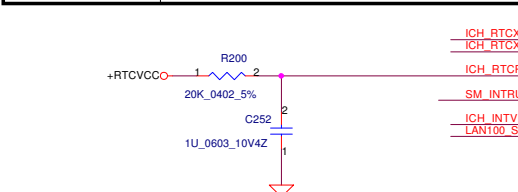
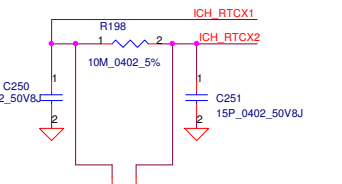
Avoid Panel display garbage after power on.



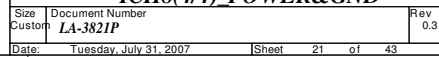
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				Size	Rev 0.3
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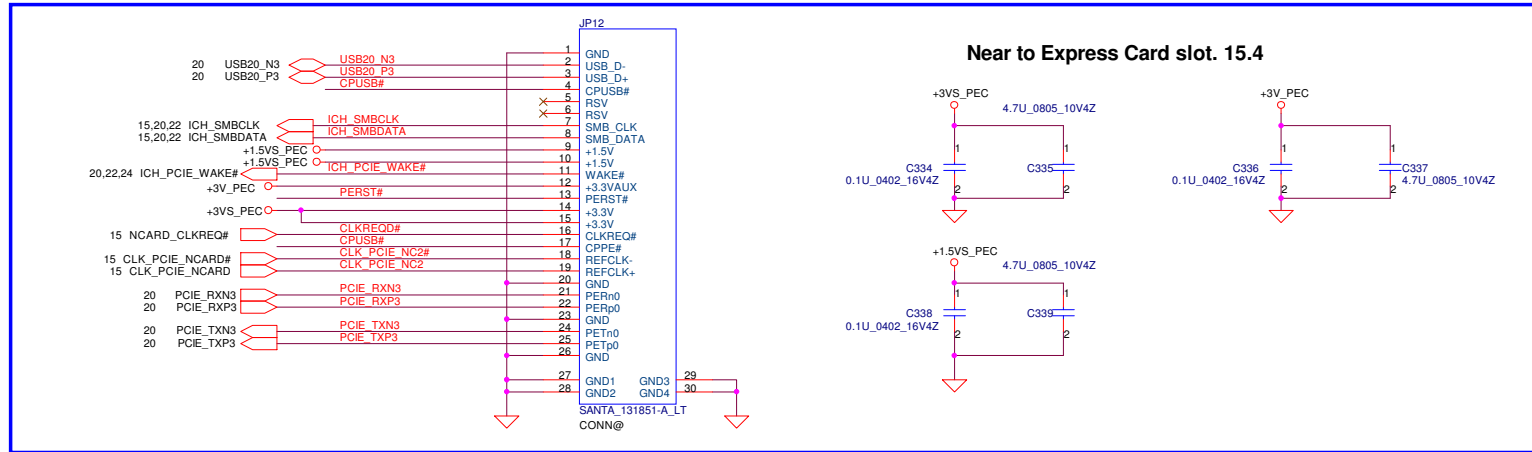


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Issued Date	2006/02/13	Deciphered Date	2006/03/10
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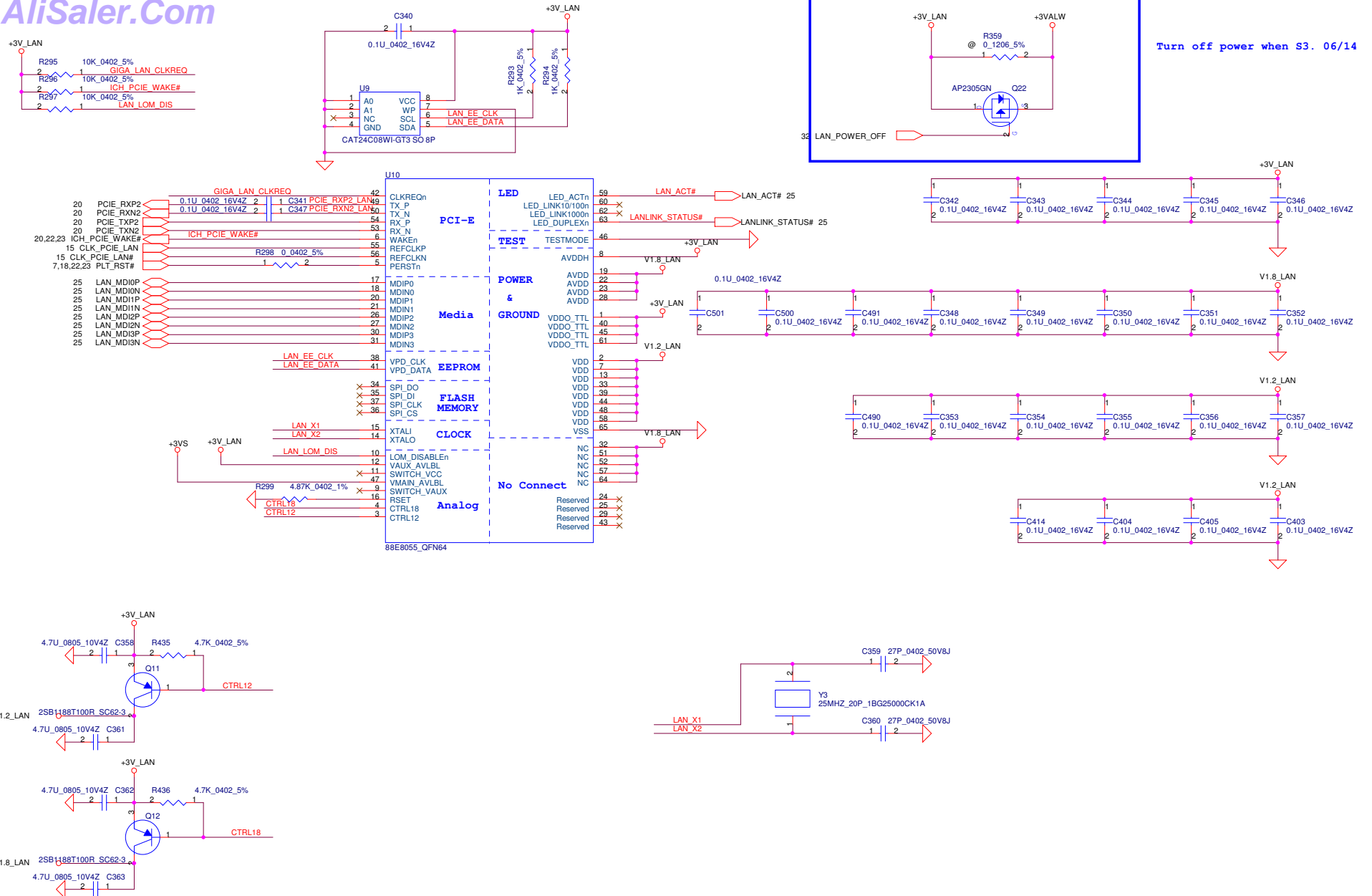




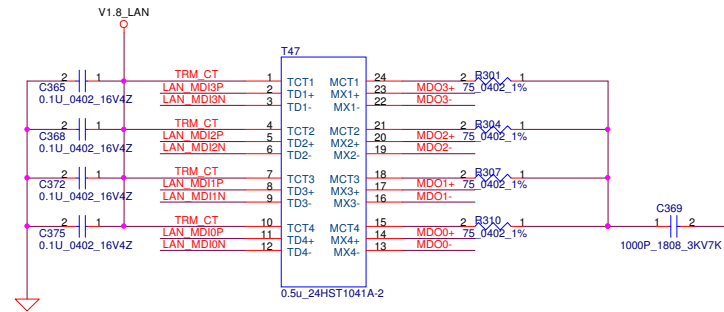
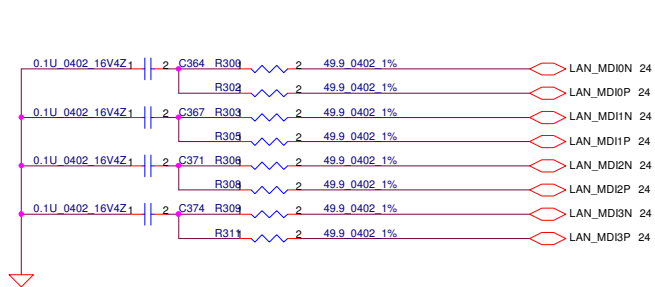
**Near to Express Card slot. 15.4**



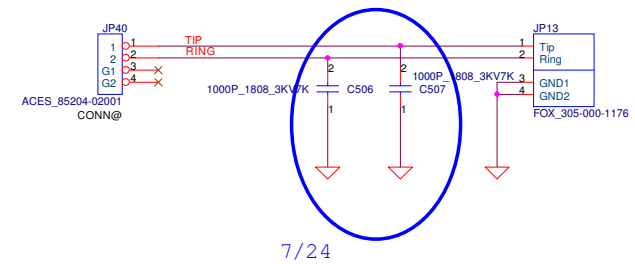
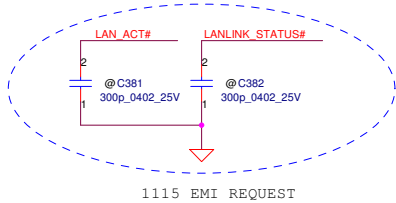
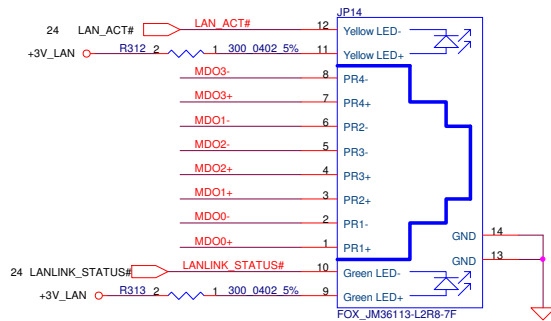
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>Express Card</b>	
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title	Rev 0.3
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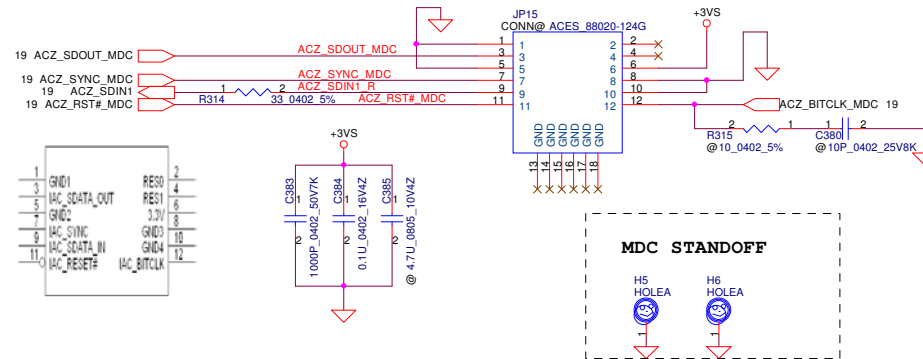
Note: MDO[3..0]+/- signals should route to JP13 first then to JP30.



RJ11

## MDC 1.5 Conn.

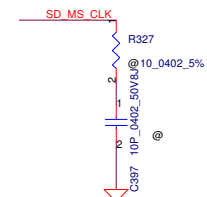
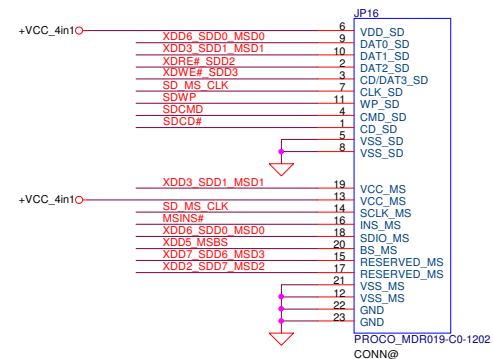
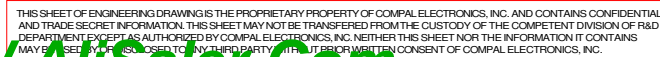
Change type 4/25

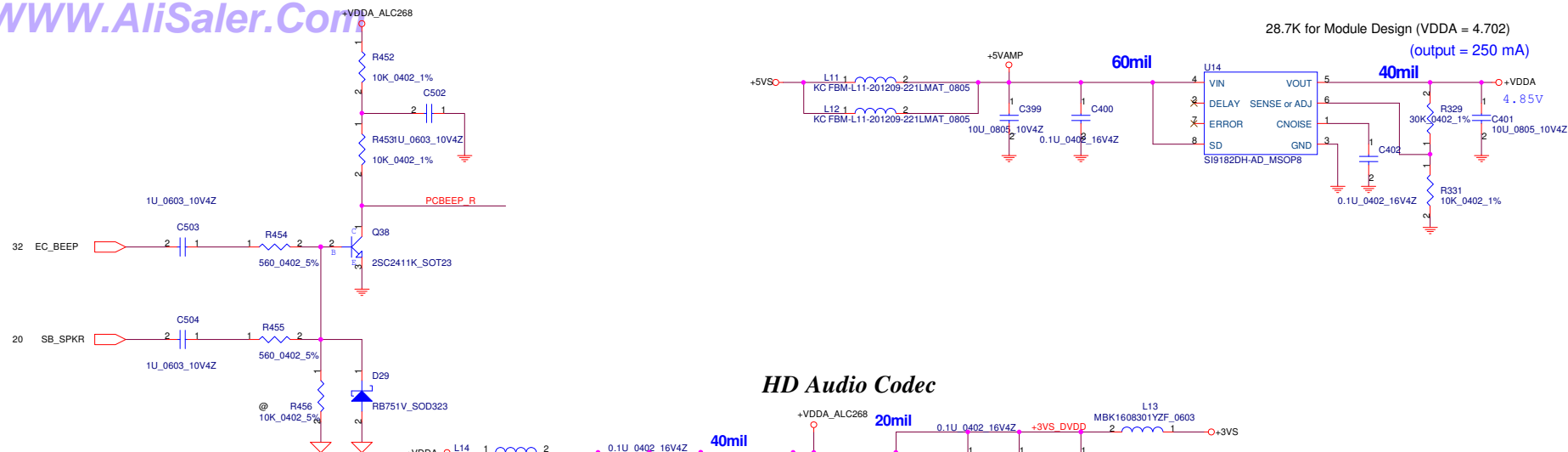


### MDC STANDOFF

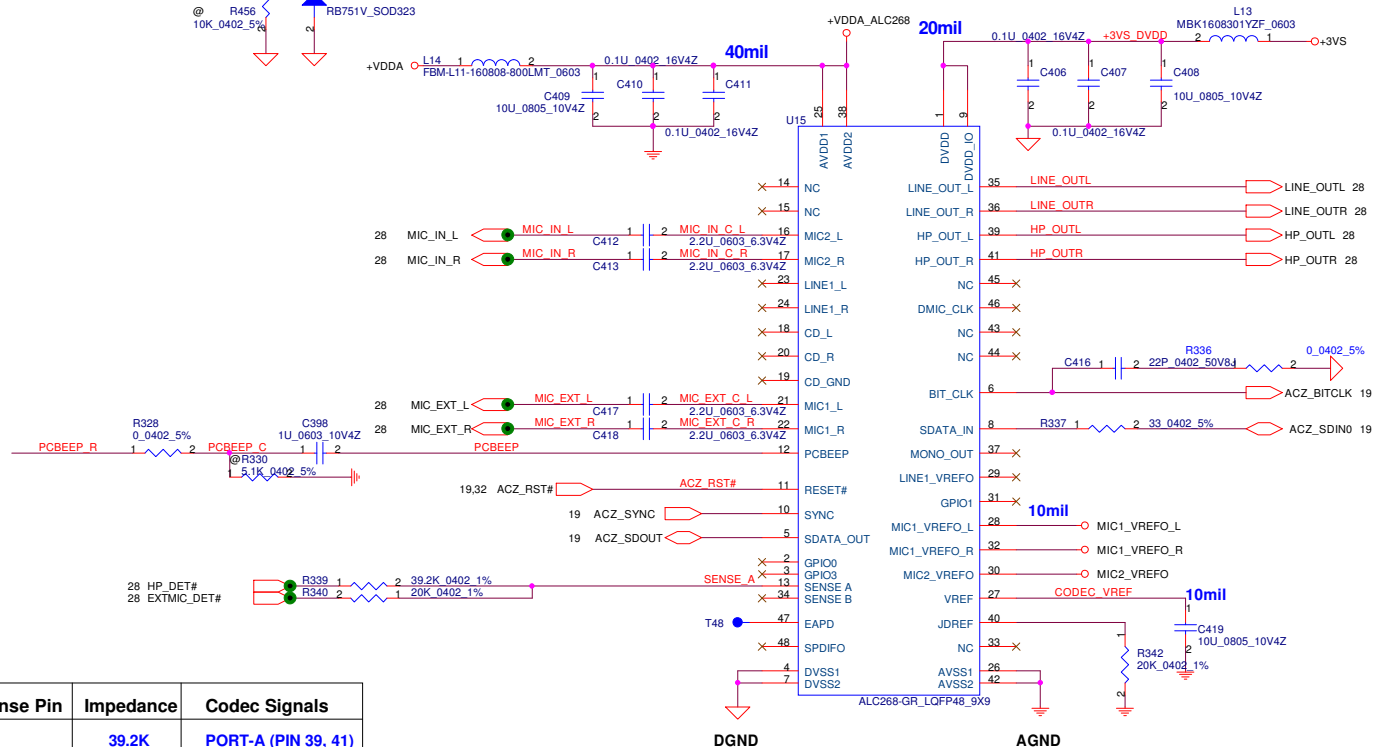


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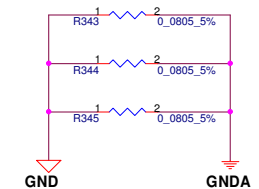




### HD Audio Codec



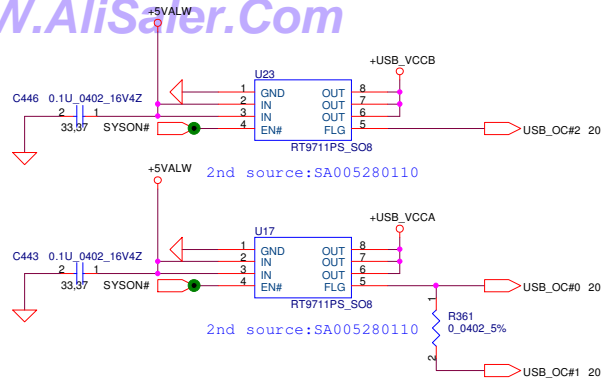
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)



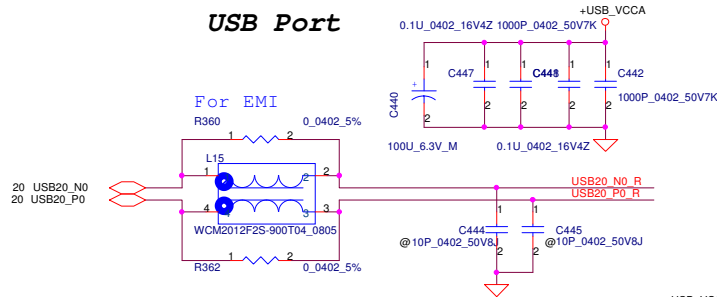
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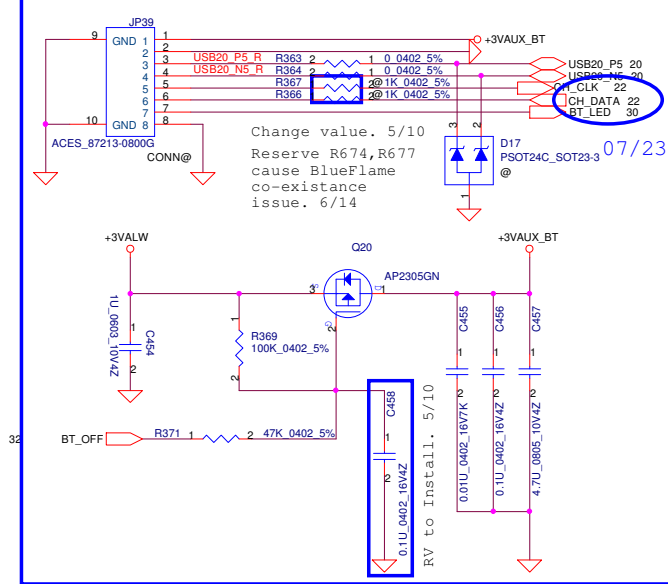
**WWW.AliSaler.Com**



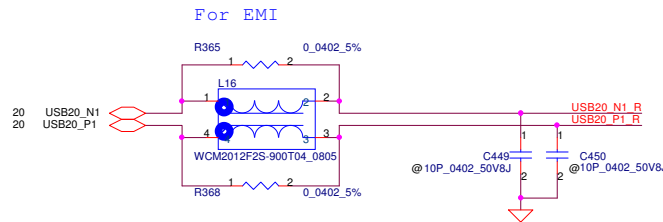
## USB Port



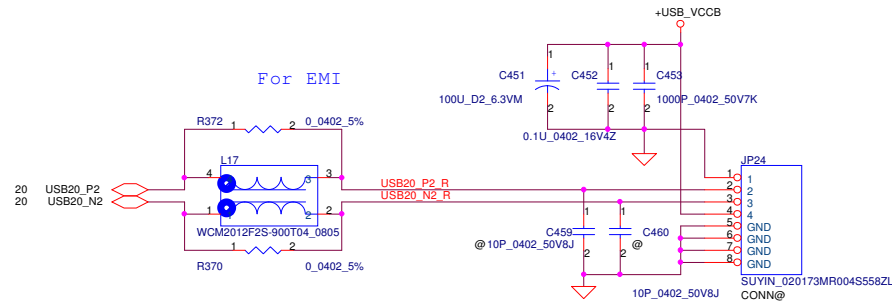
## BT Connector



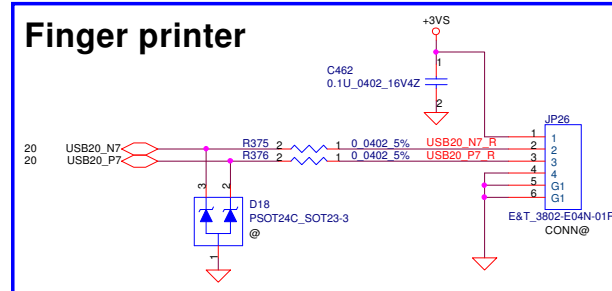
## For EMI



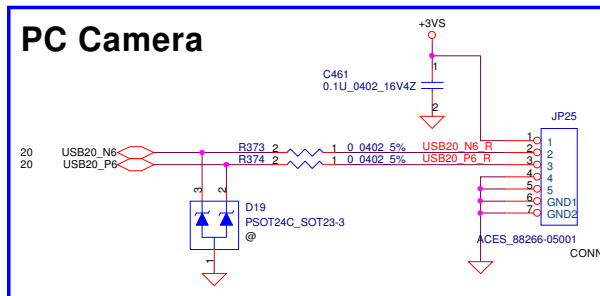
## For EMI



## Finger printer

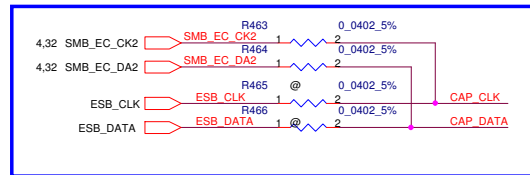
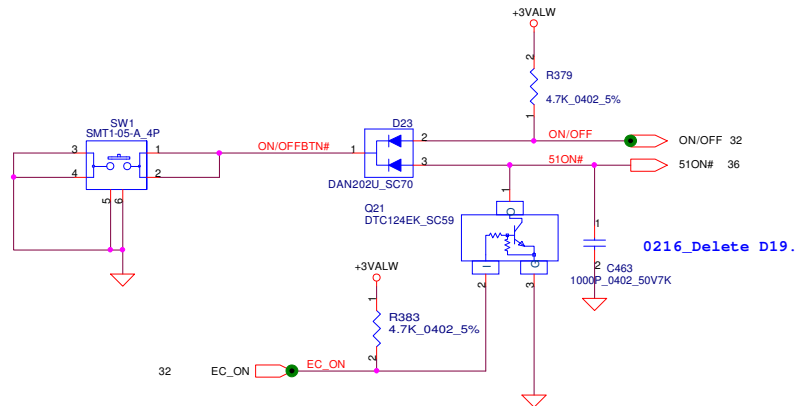


## PC Camera



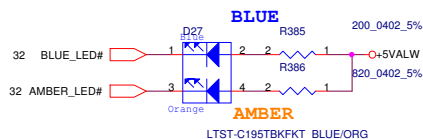
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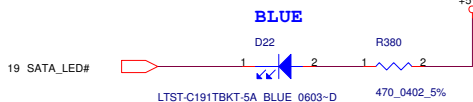


06/15 Change pin define for try ENE cap bottom

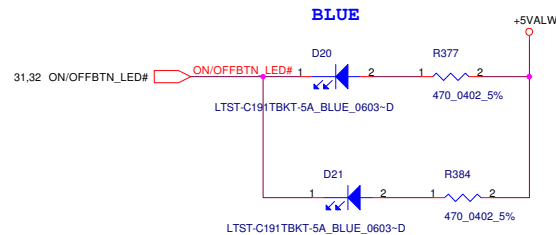
### Battery Charge LED(Left 2)



### HDD LED(Left 3)

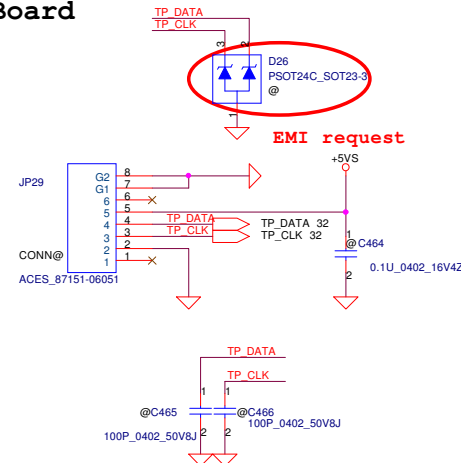


### POWER LED1

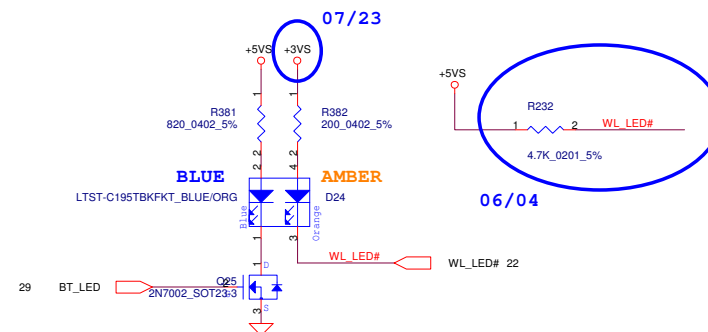


### POWER LED2

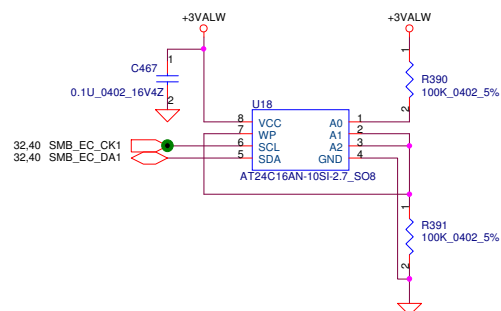
### T/P Board



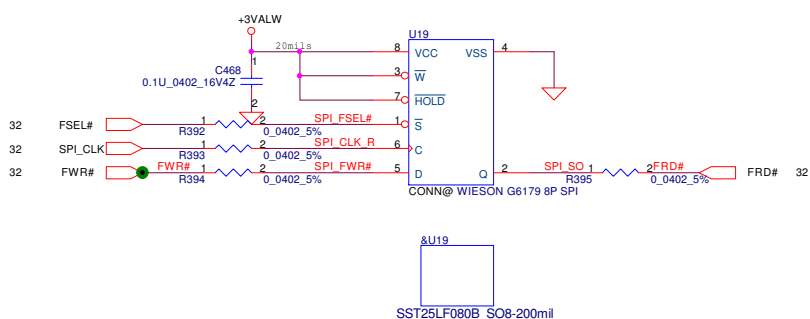
### Wireless ON Amber Bluetooth ON Blue



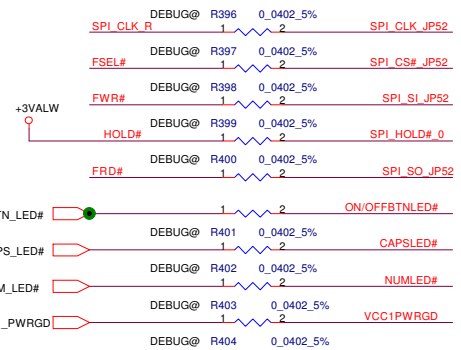
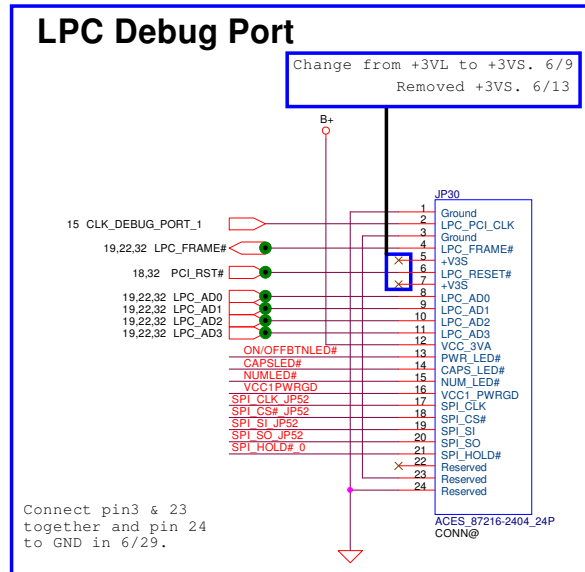
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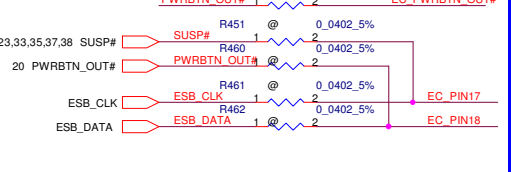
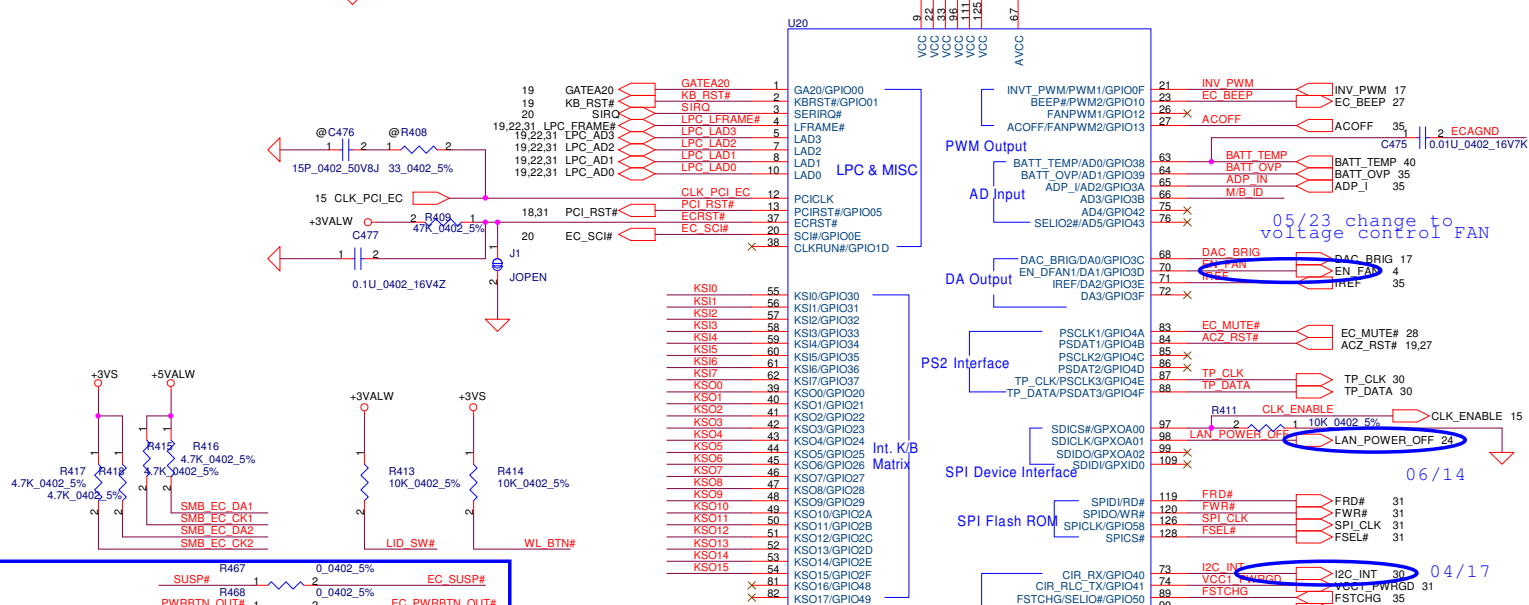
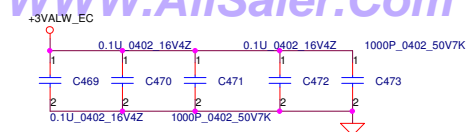
SPI ROM



B-Test remove SPI ROM socket



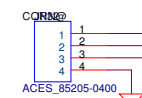
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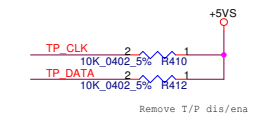
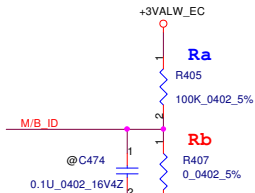
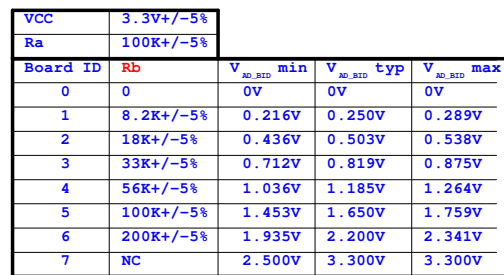
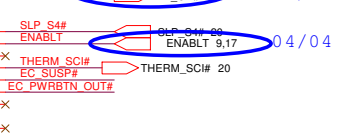
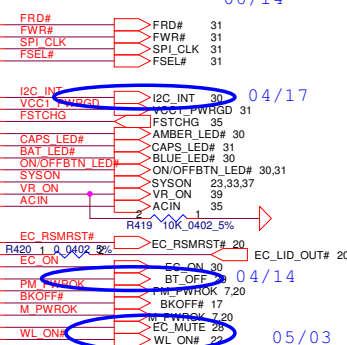
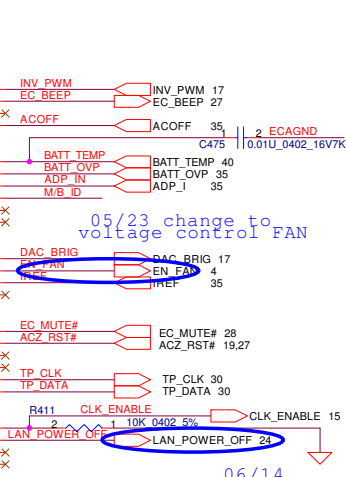
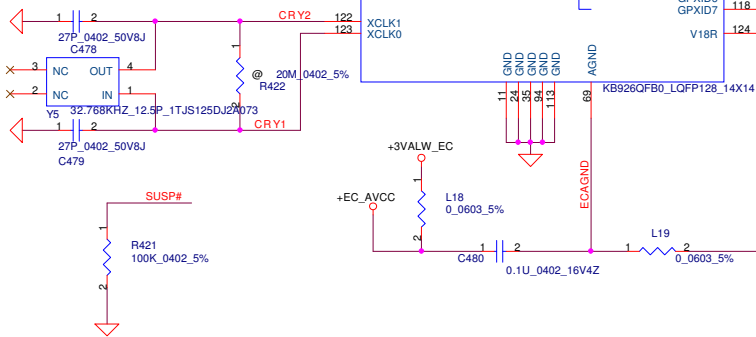
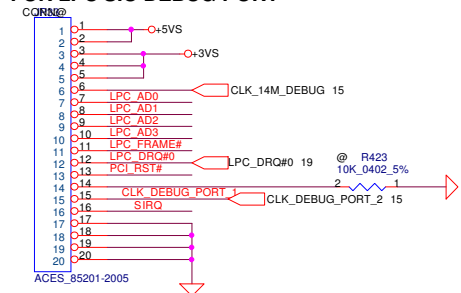
```
/15  Change pin define for try ENE cap bottom
```

05/23 change to  
voltage control FA

EC DEBUG port

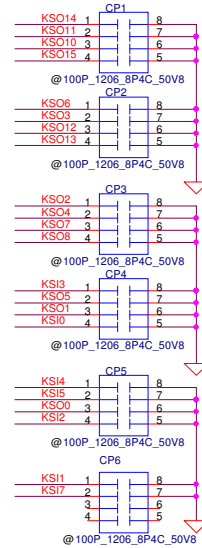
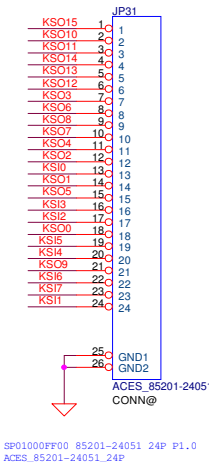


**FOR LPC SIO DEBUG PORT**



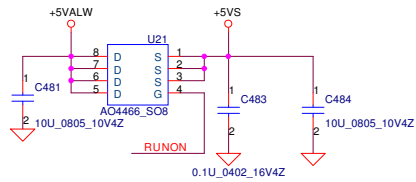
05/23 EC request

For EMI

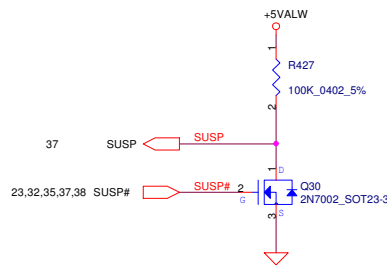
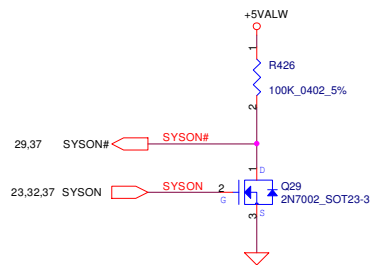
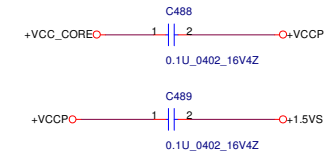
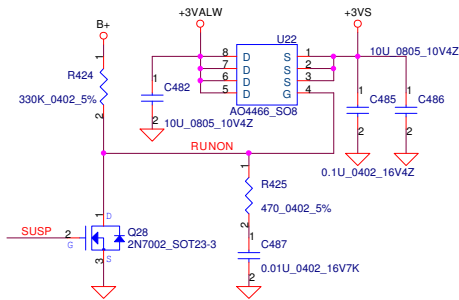


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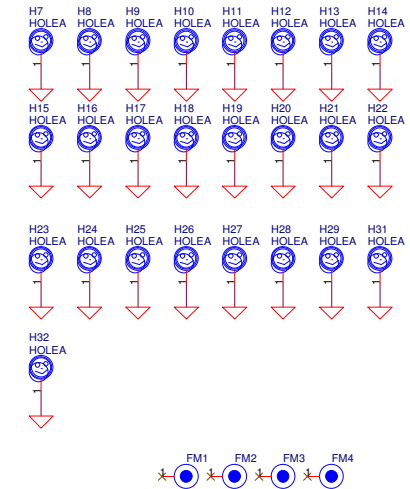
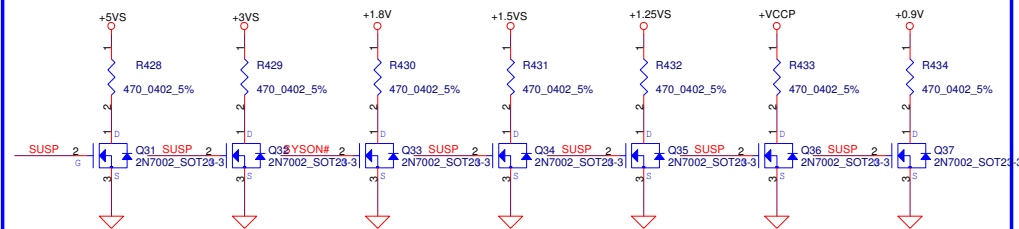
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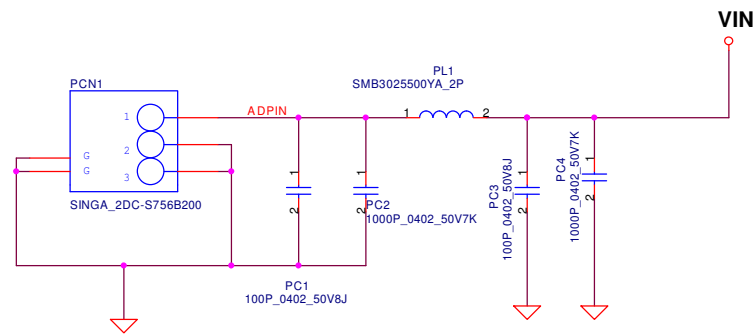
### +3VALW to +3VS Transfer



### Discharge circuit

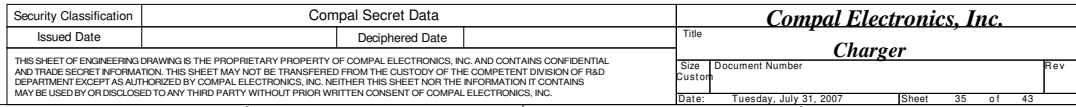


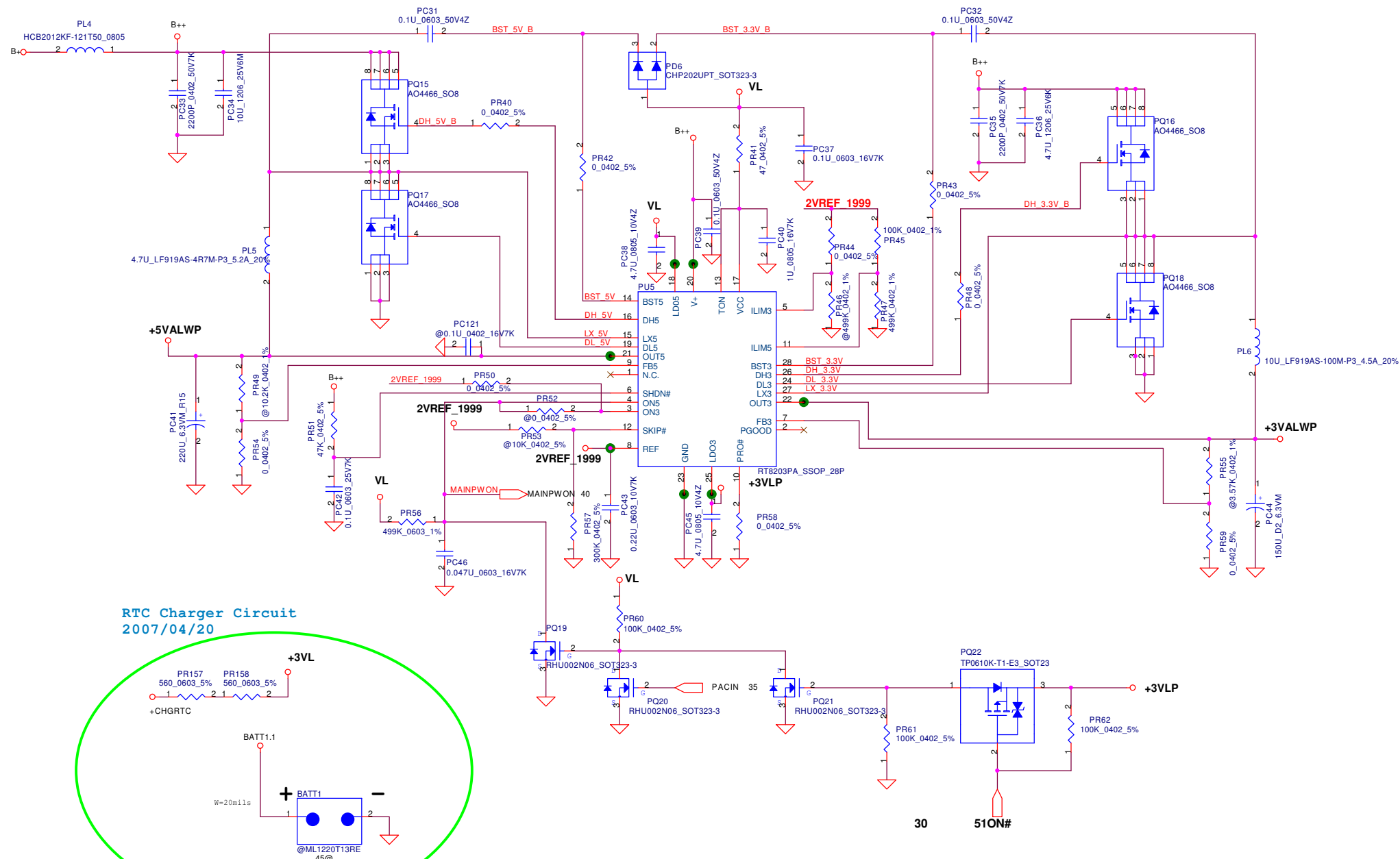
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				Date: Tuesday, July 31, 2007	Sheet 34 of 43

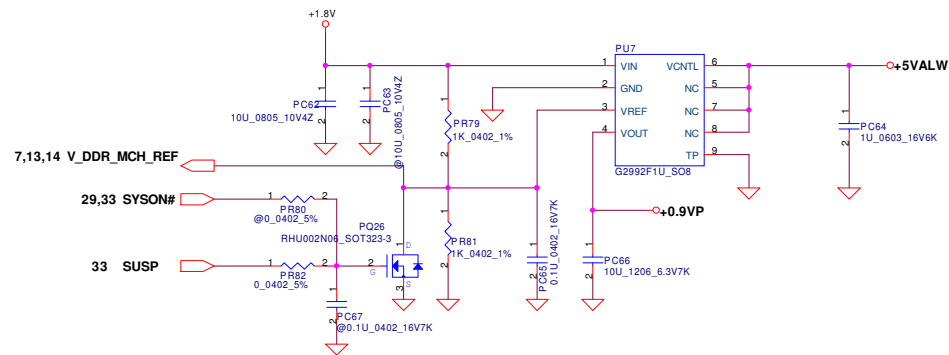
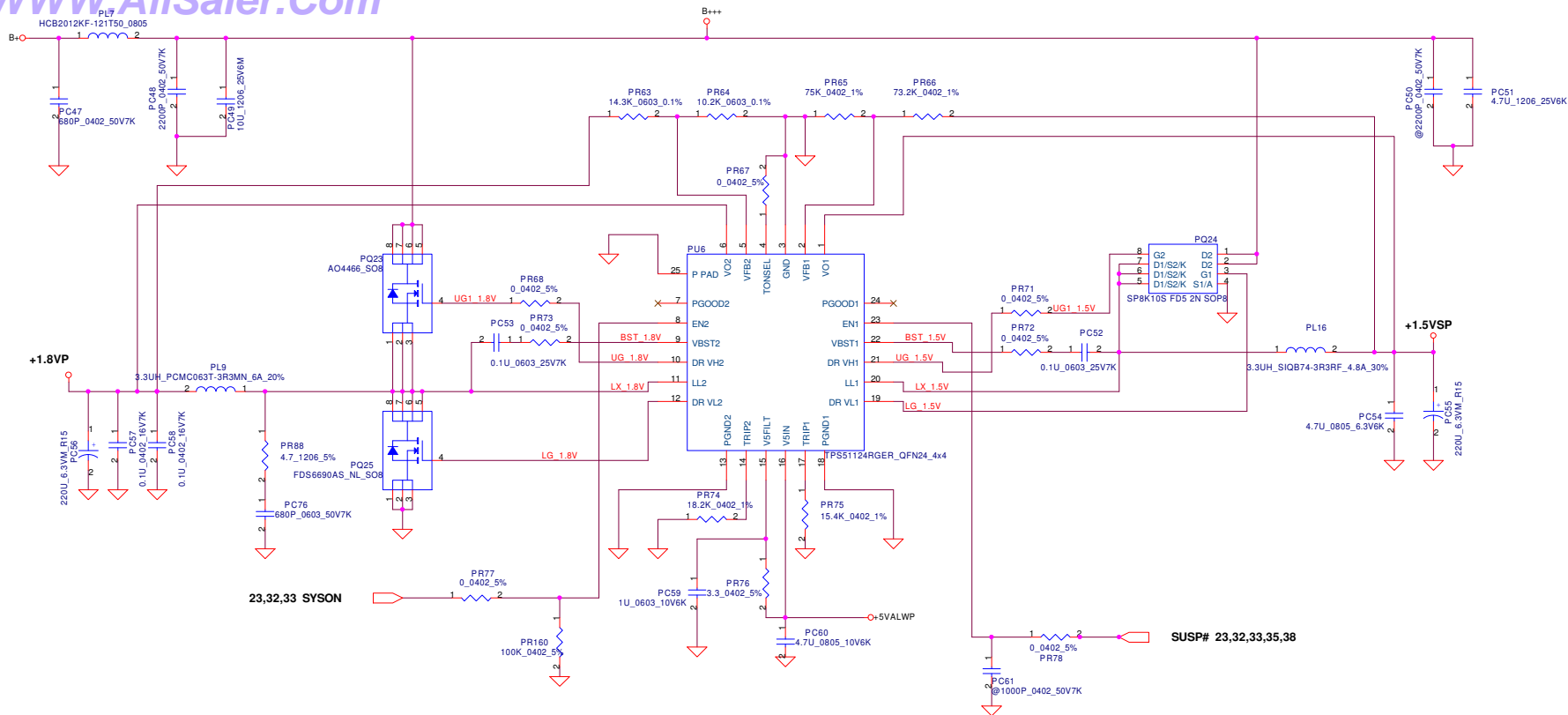
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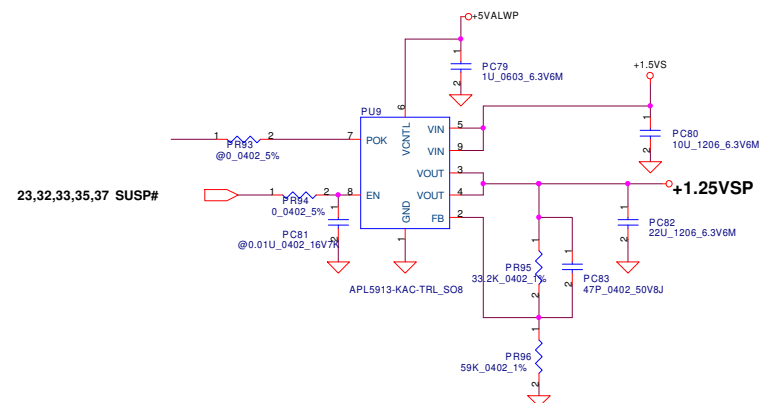
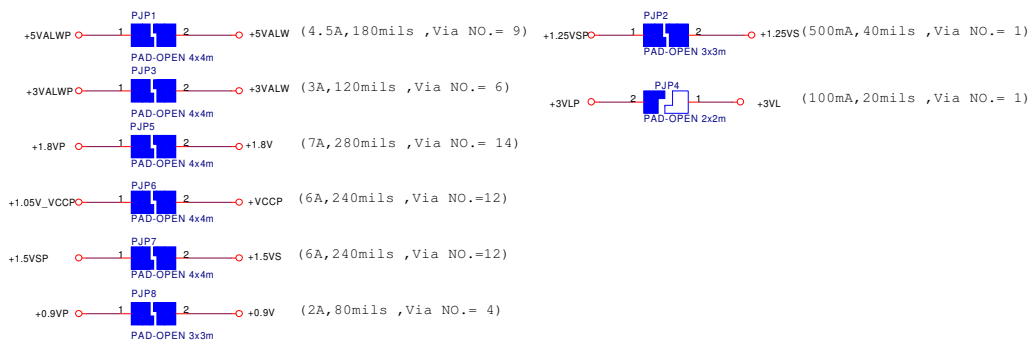
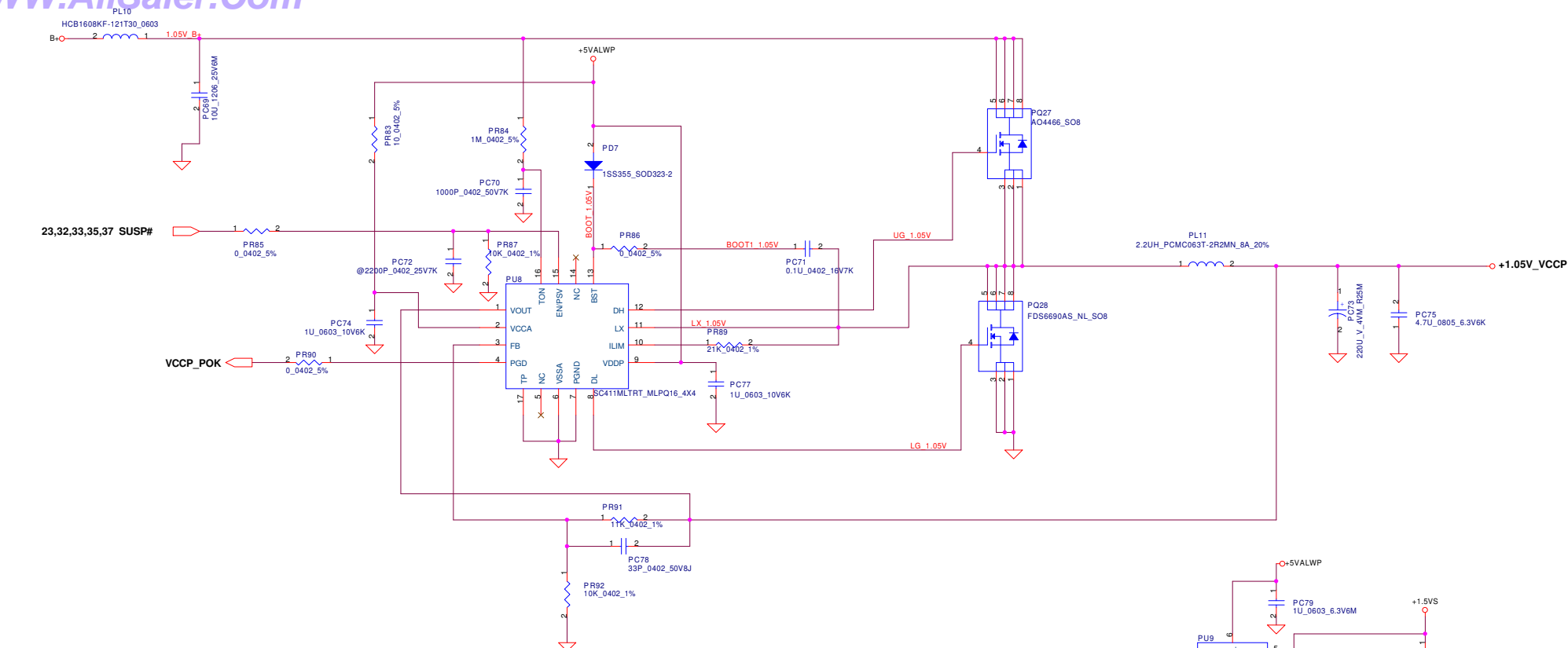


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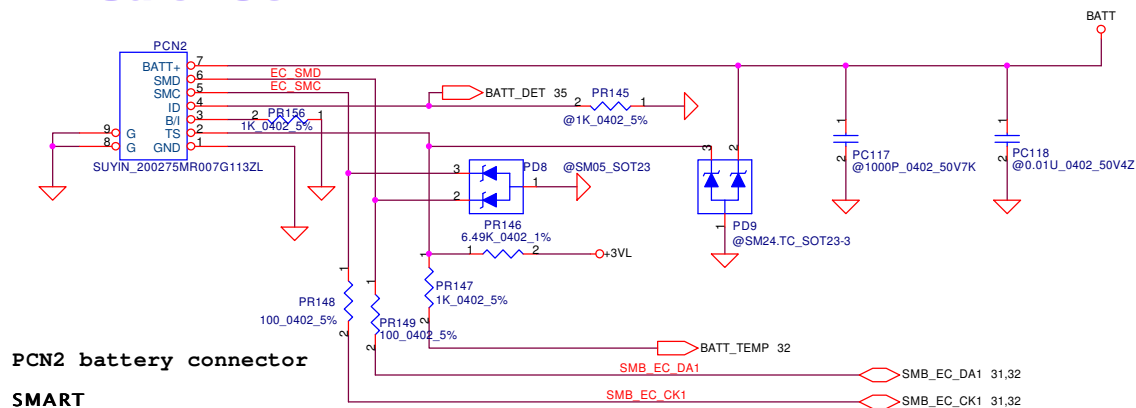


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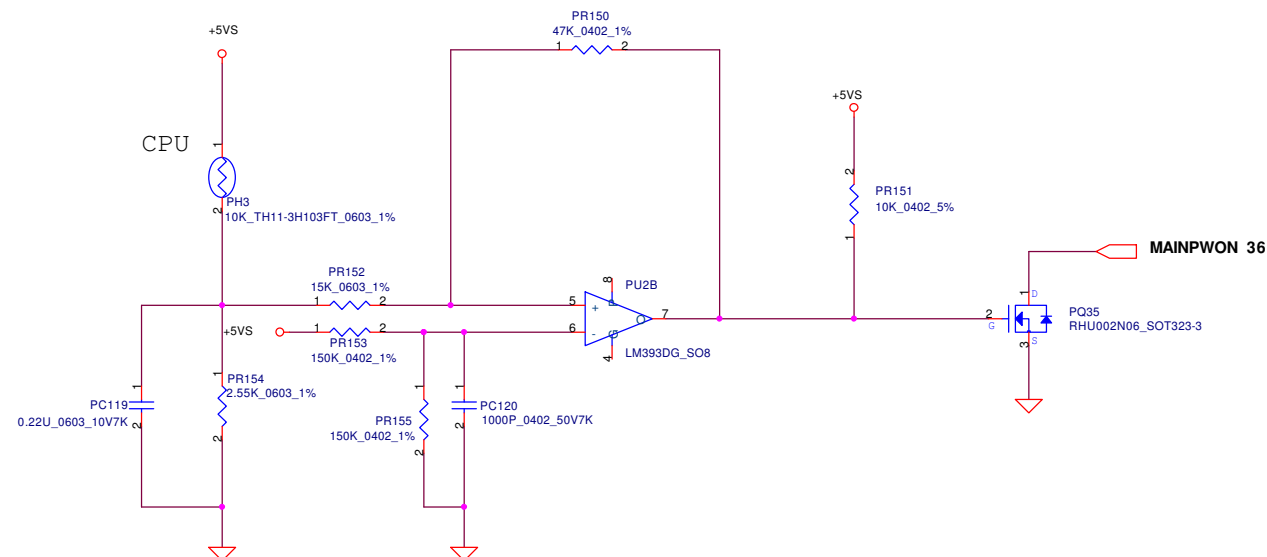


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**PH3 under CPU botten side :**  
CPU thermal protection at 90  $\pm$ 3 degree C  
Recovery at 47  $\pm$ 3 degree C



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Item	Reason for change	PG#	Modify List	Date	Phase
1	RT8203 crosstalk issue	37	add PC121 and 0.1uF	2007/05/24	SI
2	PU6 pin8 add a resistor to GND	38	add PR160 100K_ohm	2007/05/24	SI
3	remove PL15	36	remove PL15	2007/06/12	SI
4	EMI request	39	add PC122,PC123,PC124,PC125,PC126,PC127,PC128	2007/07/23	PV
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					

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Item	Reason for change	PG#	Modify List	Date	Phase
1	EC team request	32	ACIN add 100P (C505) to GND	2007/05/30	SI
2	Change Board ID	32	R407 from 0 Ohm to 8.2K,R405 install 100K	2007/05/30	SI
3	USB power switch fail	29	U23 & U17 change pin 4 from SLP_S5# to SYSON#	2007/05/30	SI
4	FAN use voltage control	4	del U2,Q1;add U24,C13 for 3 pin FAN	2007/05/30	SI
5	USB JP24 fail	29	Change pin define	2007/05/30	SI
6	Speaker output fail	28	Add R457,R458,R459 for Line_out	2007/05/30	SI
7	MS Pro fail	26	Add MS_D1,MS_D2,MS_D3 net	2007/06/06	SI
8	WLAN LED fail when disable WLAN	30	Add R232 pull high +5VS	2007/06/06	SI
9	+3VALW leakage	30	Del R387	2007/06/06	SI
10	Capacitor board fail	32	Add net CAP_RESET for Capacitor board reset	2007/06/06	SI
11	XDP fail	15	XDP clock share in robeson card	2007/06/06	SI
12	LAN power consumption is too large when S3	24	Add Q22	2007/06/14	SI
13	RJ11' cap is duplicate MDC module.	25	Delete C378,C379	2007/06/14	SI
14	Reverse some resister for tring ENE cap board	30 32	Add R460~R468,R451	2007/06/14	SI
15	+LCDVDD over current when diplay.	17	Change R163 from 47K to 100K Change C248 from 0.1U to 0.22U	2007/06/21	SI
16	LAN fail	24	Change JP14 pin define	2007/06/06	SI
17	WLAN LED (Amber led) issue	30	WLAN LED need change from +5VS to +3VS	2007/07/23	PV
18	030 project Bluetooth module issue	29	Swap pin5 & pin7	2007/07/23	PV
19	change Cap board LED supply voltage	30	from +3VS to +5VS	2007/07/23	PV
20	CMOS timing can't reset	19	SHORT PAD (CLRP3) connect between +RTCVCC and GND	2007/07/23	PV
20	EMI issue (CPU core)	5	add C43 & C44 (330U)	2007/07/23	PV
21	EMI/ESD issue (XDO connector)	4	delete XDP connector	2007/07/23	PV
22	EMI/ESD issue (RJ11 connector)	25	add 1000P at RJ11 RING & TIP	2007/07/23	PV
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